OPTOMOTIVE

Spinosaurus

Pyramid Imaging

High-speed Intelligent FPGA-based camera family:

Real Time Vision Platform

Preliminary

Product Brief v1.0

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Spinosaurus, highly customizable and user-programmable FPGA based high-speed smart cameras, is a high-end FPGA camera with a Xilinx Zynq FPGA and high speed imaging sensor and 10 Gigabit Ethernet. It includes high-performance ARM system-on-chip (SoC) technology, combined with turbocharged industrial SONY imaging sensor.

With high performance FPGA system-on-chip (SoC) technology, Velociraptor camera family opens new dimensions in computer vision. It is global shutter industrial camera with incredible frame rates and open FPGA architecture. With FPGA processing power the image processing algorithms can run in real time on the camera. Just add your imagination.

Spinosaurus includes full customizable and user-programmable open reference design for high-speed FPGA based camera and application development system. Its emphasis is on an open hardware-software development model, high-frame rates, real-time image processing on FPGA and modern graphical user interface support on the PC side.

A suite of versatile and high-performance tools for Xilinx Zynq Ultrascale+ SoC FPGA, is used to develop algorithms and process data in real-time. Images are acquired by SONY PREGIUS GEN3 sensors with SLVS-EC v1.2 interface (8x 2.3 Gbps) achieving brilliant image at very high speed. The on-board 4GB LPDDR4 memory with 9.6GB/s of bandwidth enables usage of complex buffered image processing.

The reference design can be easily edited with standard Xilinx Vivado tools. OptoMotive's custom IP cores seamlessly integrate inside the Xilinx Vivado toolchain. Large portion of FPGA (PL) is free for a programming and development of new algorithms, or implementation of additional IP cores. The 1.2 GHz Dual Core ARM Cortex A53 Programmable Subsystem runs

Linux OS with custom made EVO control and streaming stack (including Zero-copy TCP/IP stack). The SoC also includes dual 600MHz Cortex R5 processors which are free for user data processing. User applications or custom data post-processing can easily be added to existing design.

Versatile and affordable, in all possible ways!

Key camera features:

- Turbocharged industrial SONY PREGIUS GEN3 sensors, Colour (Bayer filter), Monochrome
- User programmable and reconfigurable FPGA with Quad ARM processor Zynq Ultrascale+
- Freely programmable
- 600 Gbps FPGA platform IO bandwidth
- Possible interfaces: 10/40GigE, USB3.0, 4x PCIe, DisplayPort
- Exploits maximal capability of imaging sensor
- 12 lanes Sony SLVS-EC v2.0 ready (5Gbits)
- High speed H.264 CODEC
- Neural network inference acceleration
- User programmable imaging pipeline
- 10 Gigabit Ethernet for fast data transmission
- Delivered in CNC housing or OEM version
- Firmware can be upgraded to add new features

Targeted to:

- **Laser triangulation:** with ready-made PEAK detector on-board image processing core
- **Motion capture:** with ready-made Blob detector or Running Length Encoder (RLE) on-board image processing core
- **Industrial process automation:** to count, detect, check, verify, read, inspect and test different products, levels, components, etc. at incredible speed
- **Industrial quality control:** to inspect defects, cracks or surface blemishes, size, position, dimension and colour, foreign objects, quality.
- General R&D

Options:

- Stereo remote head
- Remote SFP for OEM
- C-mount housing (IP67 option)
- 3D multiline laser triangulation core
- BLOB detection core
- Running length image compressor

Specification table

Camera Family		Spinosaurus				
Camera model		0.5	2.0	2.8	1.7	7.1
imaging sensor	Model (SONY)	IMX426	IMX422	IMX421	IMX425	IMX420
	Monochrome (M) Bayer color (C)	M or C	M or C	M or C	M or C	M or C
	Diagonal mm	9.25 (1/1.7")	9.25 (1/1.7")	10.97 (2/3")	17.55 (1.1")	17.55 (1.1")
	Active pixels H x V	816 x 624	1632 x 1248	1944 x 1427	1608 x 1104	3216 x 2208
	Frame rate (Full frame)	1590 FPS	470 FPS	408 FPS	660 FPS	200 FPS
	Pixel size	9 µm	4.5 µm		9 µm	4.5 µm
	Dynamic range	86 dB	80 dB		86 dB	80 dB
	ADC resolution	8/10/12 bit				
	Analogue Gain	0-48dB at 0.1dB step				
	Region of interest	YES, with 16 pixel increments				
	Shutter type	Electronic Global Shutter				
	Shutter time	5 us – 90 s				
	Pixel clock speed	1.9 Gpix/s (16 pixels @ 119 MHz)				
	Exposure	Linear, 3Slope High Dynamic Range				
Features	Pixel correction	Dead pixel correction and Programmable LUT				
	Trigger modes	Free running, trigger, overlap, pulse width				
	Trigger features	Delay 0 – 1000 ms, LP Filter 1.5Hz - 100 kHz				
	Shutter resolution	1.56 us				
Processing	FPGA	Xilinx Zynq Ultrascale+ ZU4CG or ZU7EV				
	Free FPGA %	Up to 50%, most of 728 slices of DSP are free.				
	Volatile memory	2 GB LPDDR4 with 9.6 GB/s bandwidth				
	Non-volatile memory	64 MB QSPI flash, 8 GB eMMC				
Mechanical	Lens mount	C-mount (1" 32G thread)				
	Temp range	0 - 50°C				
	Mass	TBD				
	Protection	Up to IP67 with housing				
	Housing material	CNC-machined aluminium, anodized				
	RoHS	RoHS compliant				
	Fixing holes	4 x M3 OEM / 5 x M6 on housing				
Electrical	Input voltage	DC 9-36V or 5V (OEM)				
	Consumption	up to 30W				
	IO	20x 3.3V TTL ZIF				
	IO isolation	3x IN / 3x OUT opto-isolated				
	Connectors	10G SFP+, 19 pin M16, ZIF on OEM				

|	On-board image processing	As an option (if an IP Core is integrated)
Functionalities	Open reference design	Yes
	Open architecture	Yes
	Software	Compatible with OptoMotive EVO software (full source included)
	Operating system	Windows XP, Windows 7, 64bit or 32bit
	Development tools	Xilinx Vivado/SDK version 2018.2 or later. Microsoft Visual Studio 2017
Standards	CE	EN55022, class A EN61000-4-2 EN61000-4-3 EN61000-4-4 EN61000-4-6
	FCC	Part 15, class A
	RoHS	Compliancy as per European directive 2002/95/EC

Mechanical drawings

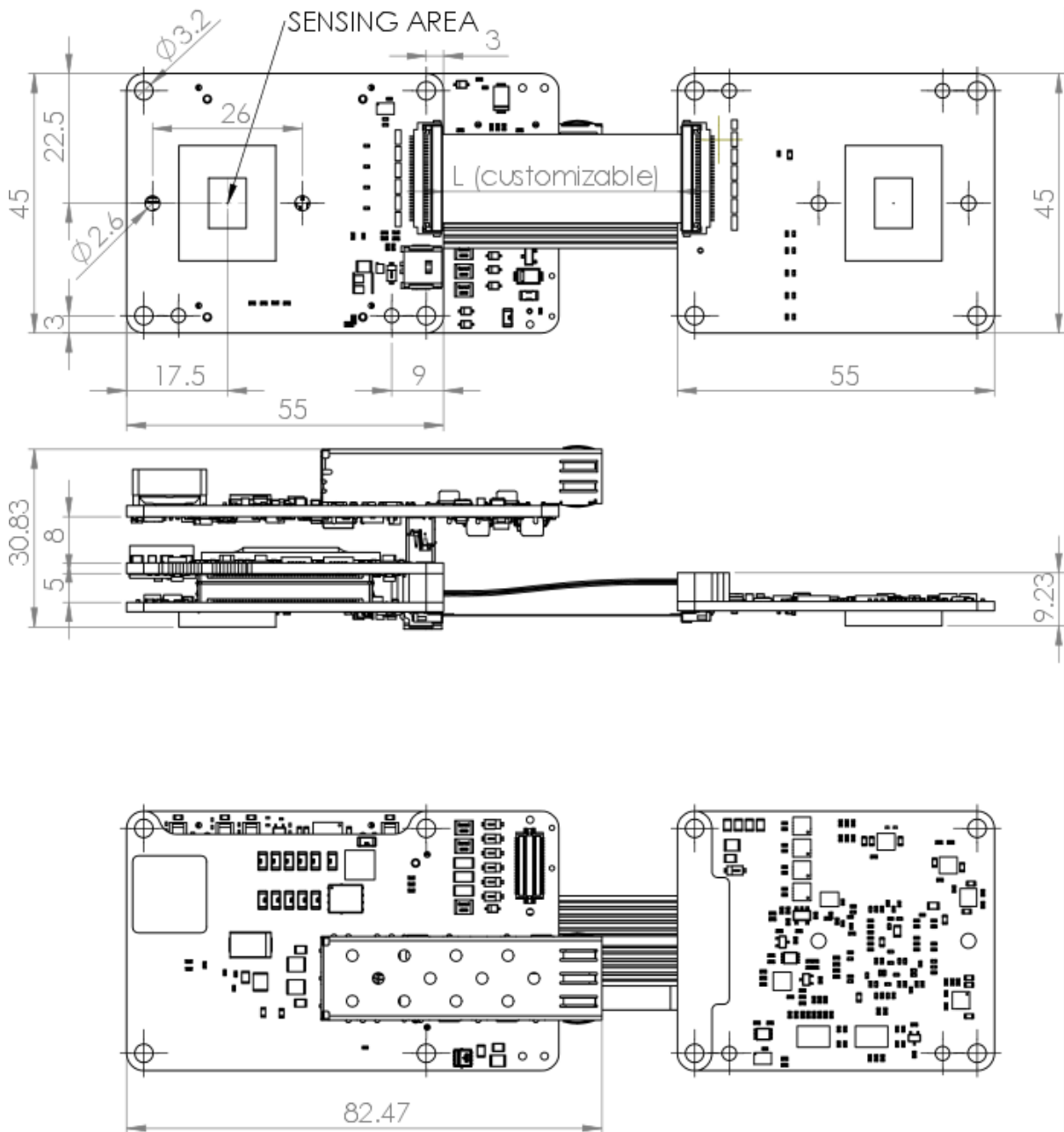 STEP 3D model available on request, C-mount OEM version is also available

Spinosaurus, OEM, Remote SFP version
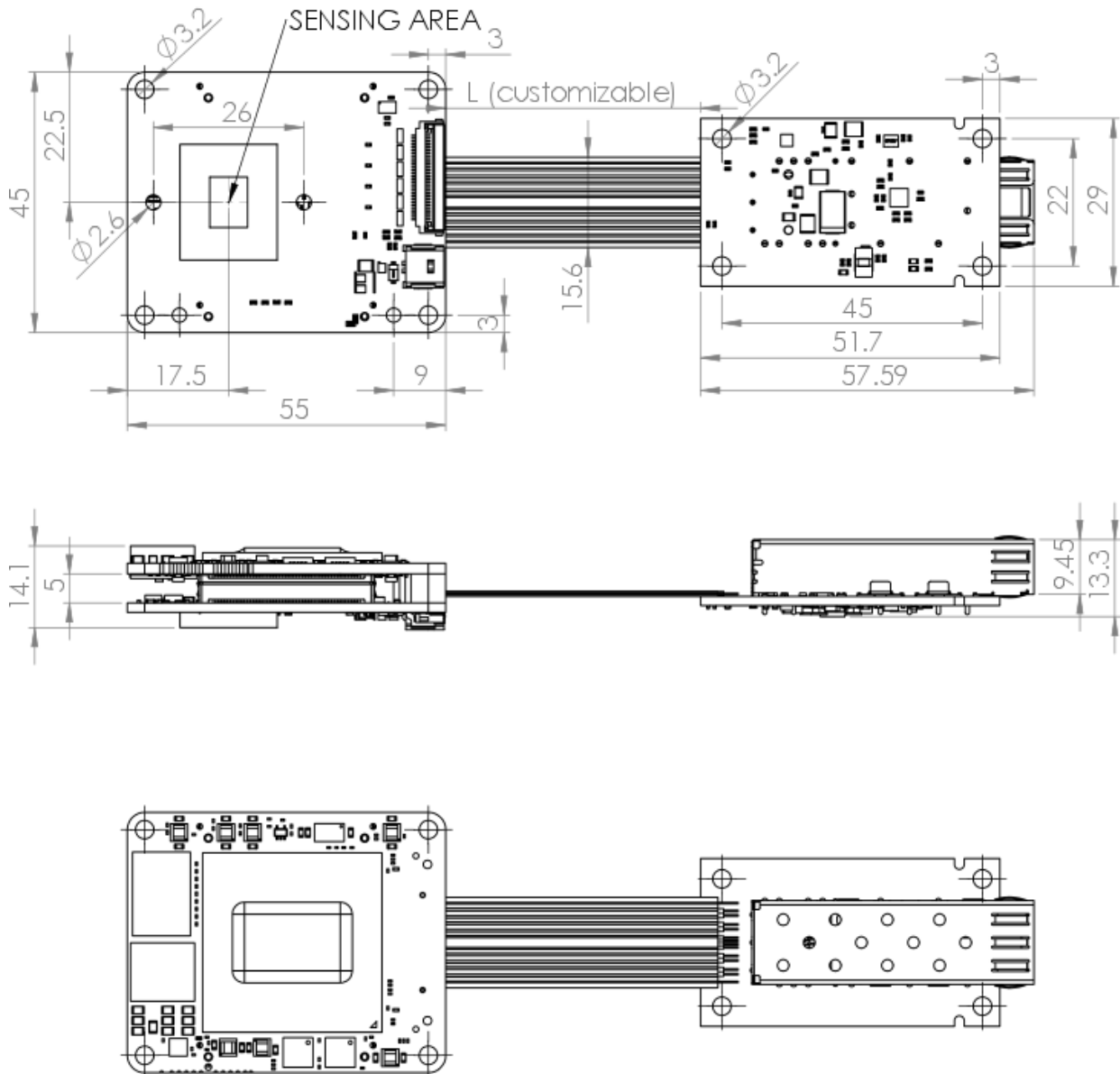
Spinosaurus, OEM, Triboard version
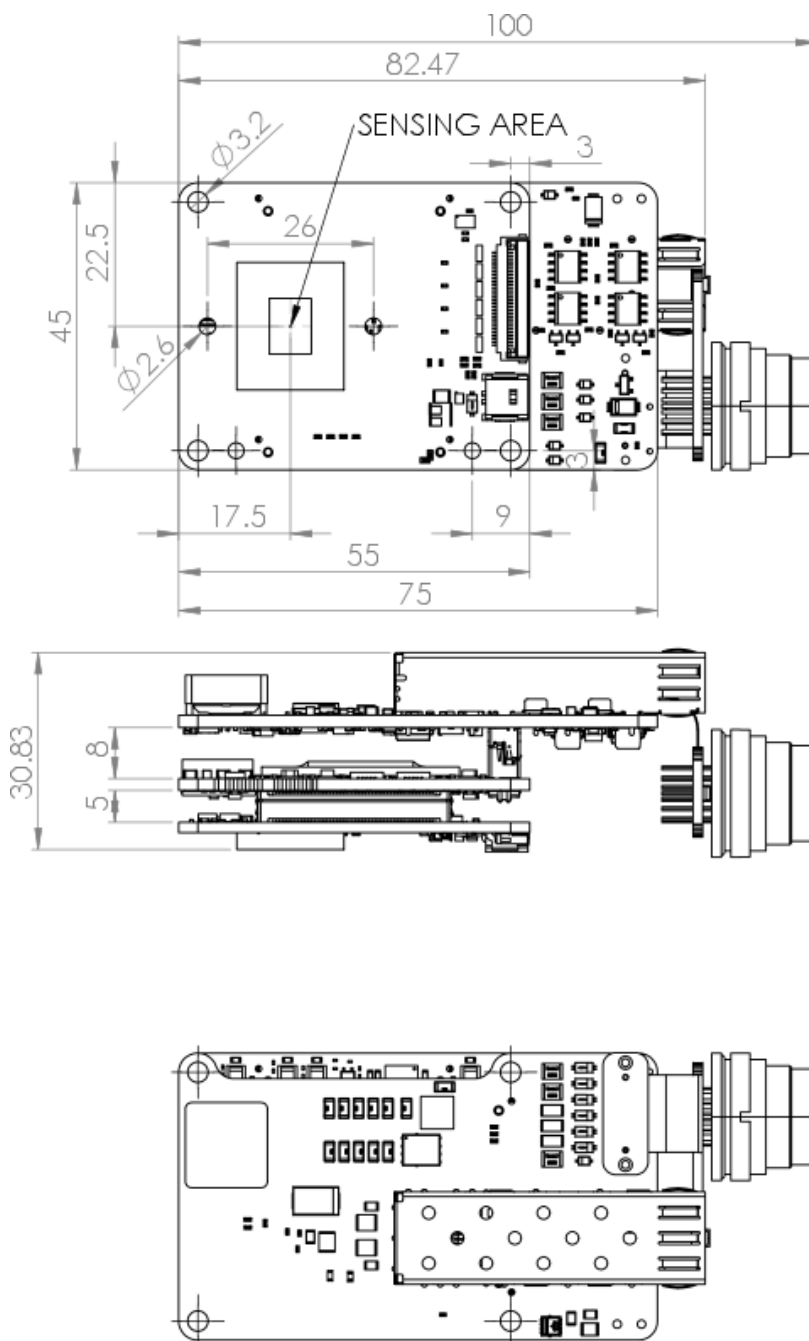
Spinosaurus, OEM, Stereo version

Spinosaurus in housing (IP67 optional)

TBD

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