PHOENIX-DIG24 PC/104-PLUS CAMERA LINK

HIGH PERFORMANCE/HIGH SPEED DIGITAL FRAME GRABBER

- Base Camera Link Configuration.
- PC/104-Plus form factor.
- 32-bit 33MHz PCI support in 3.3V & 5V signalling environments.
- Maximum PCI burst rate of 133Mbytes/sec.
- Supports digital areascan / linescan cameras.
- Accepts multi-tap & multi-channel camera formats, including line and pixel interleaved.
- Maximum pixel clock of 40MHz.
- Extended temperature operation.
- Software Development Kit (SDK) supports various operating systems for rapid integration.
- v2.2 PCI and v1.1 Camera Link compliant.
- Bus mastering hardware control of scatter-gather requires 0% host CPU intervention.
- Serial port with EIA-644 signalling.
- Supports Camera Link serial comms API.
- Implements Data Valid (DVAL) for slow data rate cameras.
- Opto-Isolated, TTL and RS-422 I/O.
- Utilises software configurable FPGA technology for maximum flexibility.
- RoHS compliant.

Active Silicon
COMPUTER IMAGING PRODUCTS

OVERVIEW

Phoenix-Dig24CL is a PCI board for the acquisition of digital data from a variety of Camera Link sources, including digital frame capture and line scan cameras. It supports all the formats of Base configuration, i.e. single 8 to 16-bit data, through 8-bit RGB, to dual tap 12-bit sources.

Phoenix-Dig24CL also supports various camera tap formats, such as line interlaced - adjacent lines are output simultaneously; line offset - lines are output from different parts of the CCD simultaneously; pixel interlaced - adjacent pixels on the same line are output simultaneously; and pixel offset - pixels are output from different parts of the same line simultaneously.

ROI and sub-sampling controls are used to increase application processing speed by only storing the required data. In addition, the LUT functionality provides support for gamma correction, dynamic range cropping and binary thresholding in real time. The DataMapper further reduces the load on the host processor by mapping and packing the acquired data prior to transfer across the PCI bus. For example, the acquired data can be mapped into a suitable format and transferred directly to the graphics display, without the need for any host processing.

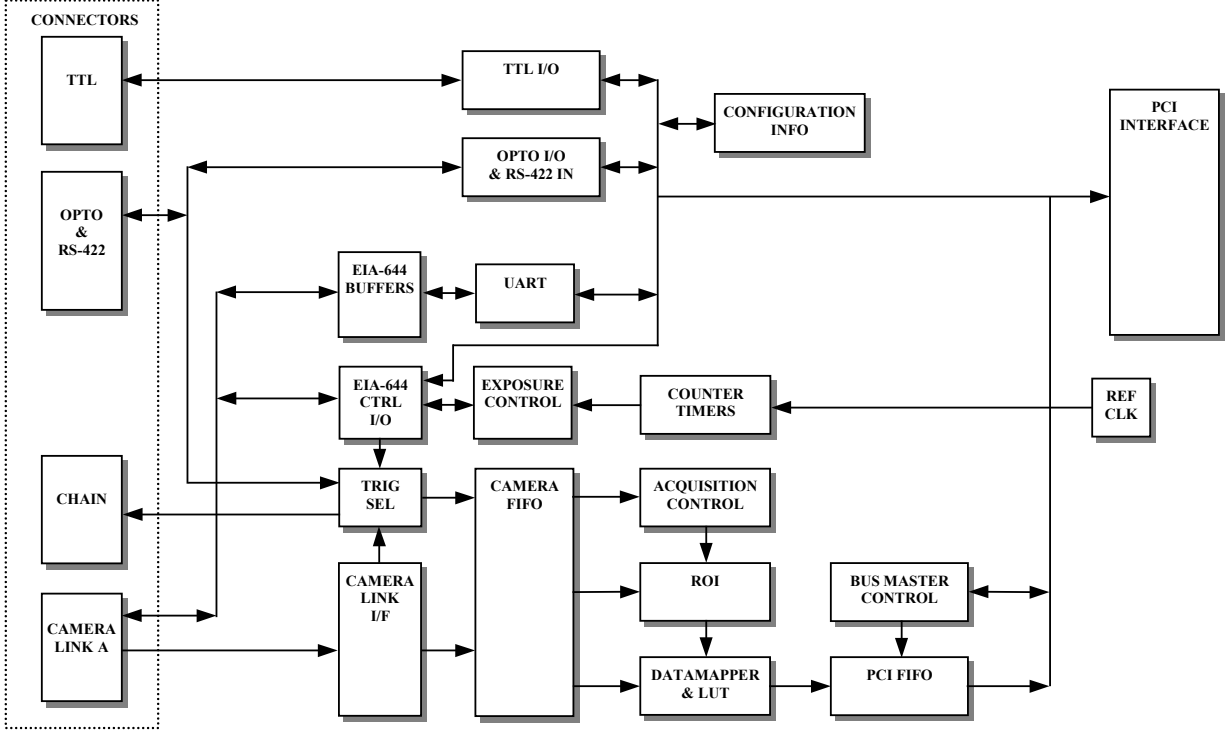
The PCI interface comprises intelligent scatter-gather hardware which reads its instructions direct from memory without any host CPU intervention. This in turn controls the DMA engine, which transfers the packed video data into any target memory which can be reached from the PCI bus. This can be system memory, graphics memory, or even other devices on the same or other PCI busses, such as DSP cards, etc.

The majority of the functionality is implemented in a single FPGA (Field Programmable Gate Array) providing a flexible solution for interfacing to Camera Link compliant sources. The FPGA implements the PCI interface, hardware scatter-gather control, PCI Initiator Burst Control (DMA), Acquisition Control, Region of Interest (ROI) and sub-sampling control, DataMapping functions, Datapath FIFOs, and Counter/Timer support. In addition, the board contains Look Up Table (LUT) functionality, a Universal Asynchronous Receiver Transmitter (UART), 4-bit opto-isolated I/O, two 2-bit differential input ports and two 8-bit TTL I/O ports.

The Software Development Kit (SDK), available as a separate item, allows rapid system development and integration. It provides comprehensive example applications and optimized libraries, and is available for a variety of operating

systems via a common API, including 32-bit Windows, Mac OS X, DOS, VxWorks, QNX and Linux. Drivers for third party applications are also available, e.g. Common Vision Blox, Image-Pro Plus, etc. As well as functions that control the hardware, the libraries include general purpose functions for the manipulation and display of images. A separate datasheet describes the SDK in detail.

SYSTEM BLOCK DIAGRAM



Note: This is a simplified block diagram that only shows the main data and control paths.

HARDWARE SPECIFICATION

Camera Clock:	***Phoenix*** supports effective clock rates from DC to 40MHz, using the Camera Link Strobe (STB) and Data Valid (DVAL) signals. For faster speeds contact your distributor.
Camera FIFO:	Data from the video source is stored in a FIFO prior to being processed by ***Phoenix***.
Acquisition Control:	The acquisition trigger control module is used to determine which video frames to acquire from the camera. The system can be configured for a single trigger event to acquire all subsequent frames, a trigger event per frame, or continuous acquisition irrespective of the trigger condition. The trigger event is programmable between level or edge sensing on one of the opto-isolated or RS-422 control inputs. When running in linescan mode, there is an additional mode that uses the active trigger input as an envelope signal. In this mode all lines are acquired whilst the trigger input is asserted. The hardware can also delay the trigger event by a fixed time period or number of lines, and allows the trigger event transducer to be located remotely from the camera.
Region of Interest:	The Region Of Interest (ROI) controls which part of the camera output data to acquire. In areascan mode, this is a rectangular region with software programmable width, height and x / y offset. Linescan mode is similar, allowing control of the width and x offset, with the height control being used to package the data into pseudo frames for subsequent processing by the user's application. ***Phoenix*** supports an additional mode (DataStream) whereby data is acquired based upon the control inputs, e.g. all data is acquired when Frame Valid (FVAL) and Line Valid (LVAL) are both asserted. This is necessary for cameras that output their own arbitrary ROIs within a single video frame, or those that vary the amount of data output on each line.
Sub-Sampling:	Software controlled hardware sub-sampling is also supported. A factor of x1, x2, x4 or x8 can be independently selected for both x and y directions, e.g. a horizontal factor of x4 and a vertical factor of x2 would acquire every 4th pixel across a line and every 2nd line down the frame.
DataMapper:	The raw camera data can be reformatted in hardware for ease of subsequent processing. For example, a mono data source can be converted into 32-bit color data, ready to be sent directly to graphics card memory, thus reducing the host processor overhead. The optimum use of system resources is determined by the user's application, e.g. packing mono data into 32-bit color reduces the host processor overhead at the expense of increasing the amount of data transferred across the PCI bus. The output formats supported include, 8, 16 and 32-bit mono, as well as 15, 16, 24, 32 and 48-bit color in both RGB and BGR ordering, thus supporting big and little endian processor formats. The data is also pre-packed into a 32-bit stream, prior to being sent across the PCI bus, for maximum transfer performance.
LUT:	A 16 bit in, 16-bit out (i.e. 65,536 by 16) LUT allows arbitrary mappings between the input data from the video source and the output data to the destination memory. This allows functions such as gamma correction, brightness, contrast and thresholding to be performed in real time in hardware on a per color or per camera basis. The LUT may also be used to shift the LSB aligned video data to MSB alignment ready for processing.
PCI FIFO:	A 1536 by 32-bit FIFO provides buffering between the camera and the PCI bus. Note that this is not a frame store; ***Phoenix*** uses high speed Bus Mastering (DMA) to transfer the camera data into system memory, and therefore the image size is only limited by the amount of memory available on the host.

Bus Master Control:	Core to ***Phoenix*** is a dedicated RISC processor and a highly optimised PCI Bus Master (DMA) engine. The RISC processor reads transfer length and destination address instructions across the PCI bus from host memory, and loads these into the PCI Bus Master engine with no host CPU overhead. The DMA engine then transfers the video data at the full PCI bus rate into host memory, thus achieving the maximum burst rate of 133MBytes/sec. When the current instruction has completed, the RISC processor optionally generates a PCI interrupt to signal that the transfer has completed, before either halting or retrieving the next instruction. The RISC processor also supports jump instructions that allow a single piece of RISC code to continuously loop without any CPU intervention.
Interrupts:	An interrupt signal is available, and can be configured via software to interrupt on a number of different events, including acquisition complete, FIFO overflow, Start/End of Frame/Line, etc.
Counter Timers:	Four 32-bit counter timers are available on ***Phoenix***. The counter timers are dedicated for the following functions: 1. Astable timer used as a line rate generator for linescan cameras, or as an acquisition trigger for areascan cameras, thus controlling the overall frame rate. The period of the astable can be set from 1µs up to 70 minutes in 1µs increments. 2. Dual monostables for generating two exposure output signals, e.g. ExSync and PRIN. Both monostables are triggered by the same software selectable event but can be programmed with different time periods, once again to 1µs resolution. This provides a flexible exposure control system. 3. Trigger delay counter used to postpone acquisition triggering by a programmable time delay or line count. This allows the acquisition trigger sensor to be mounted remotely from the camera. (Note: As the counter is non-retriggerable, subsequent trigger events will be ignored until a pending event has completed its delay). 4. A versatile event counter is provided to count a number of different events types - Lines (LVAL), Frames (FVAL) or microseconds, within a specified gate condition - Line (LVAL), Frame (FVAL), Acquisition Trigger or Entire Acquisition. The event count provides readings for both the current value, as well as the final value at the end of the previous gate condition. For example, the event counter can be configured to provide the current line number within a frame, as well as the total number of lines in the previous frame. Other uses include providing the frame period, the number of lines in the previous acquisition trigger envelope – and hence how much data there is to process, or the number of images processed so far.
Camera Control Outputs:	A 4-bit EIA-644 (LVDS) output port is provided to interface with the camera. Each bit can be individually set to a logical “1” or “0” under software control or used to drive the camera with exposure control pulses from the counter timer module. The port is on the Camera Link connector.
Opto-Isolated I/O:	4 bits of opto-isolated I/O are provided to interface to external systems. These are configured as 2 bits of input and 2 bits of output. The outputs are designed to sink up to 20mA and will withstand 24V when “off”. The inputs sense voltages between 3.3V and 24V as a logic high input. A 4.7kΩ current limiting series resistor is fitted on all inputs. The outputs can be individually set and cleared via software, controlled from the internal timer resources, or fed from other input events, e.g. acquisition triggers, etc.
RS-422 Control In:	Two 2-bit RS-422 input ports are provided to interface with other systems. They can be used to read status information from the camera, as additional acquisition trigger sources, or as inputs from shaft encoders, etc.
TTL I/O:	Two 8-bit TTL I/O ports are provided to interface with other systems. Each 8-bit port can be independently configured as all input or all output under software control. When used as outputs, each bit can source 24mA at min 2.2V or sink 24mA at max 0.55V. When used as inputs, an applied voltage of between 2V and 5V is read as a logical “1” and an applied voltage of between 0V and 0.8V as a logical “0”.

Serial Port:	***Phoenix*** is fitted with a Universal Asynchronous Receiver Transmitter (UART), containing 64-character hardware transmit and receive FIFOs (the software libraries buffer the transmit and receive data to provide larger user FIFOs). Supported formats are 1, 1.5 or 2 stop bits; 5, 6, 7 or 8 data bits; and odd, even or no parity. The baudrate can be configured with standard values from 300 baud up to 115,200 baud. ***Phoenix*** also supports software (XON, XOFF) flow control within the UART without host CPU intervention.
PC/104-Plus:	***Phoenix*** is fitted with two jumpers to set the slot number. For high reliability applications the slot setting can be made using solder bridges on special pads on the PCB. ***Phoenix*** needs to be used in a slot that supports both DMA and interrupts.
Connectors:	***Phoenix*** is fitted with the 26-way 3M MDR connector and screwlocks as specified in the Camera Link v1.1 specification. For opto-isolated, RS-422 & TTL I/O there is a 50-way 0.1" IDC header. Two 10-way 0.5mm pitch FPC connectors ("Chain") allow two ***Phoenix*** boards to be used together to simultaneously acquire from wider sources. The next section shows the pinout of the connectors.

CONNECTOR PINOUTS

Camera Connectors

Phoenix-Dig24CL is fitted with a 26-way mini-D Camera Link socket.
Connector type: 3M MDR (N10226-52B2VC) with 3M screwlocks (3341-31).

PIN	SIGNAL	PIN	SIGNAL
1	Inner Shield	14	Inner Shield
2	CC4-	15	CC4+
3	CC3+	16	CC3-
4	CC2-	17	CC2+
5	CC1+	18	CC1-
6	SerTFG+	19	SerTFG-
7	SerTC-	20	SerTC+
8	X3+	21	X3-
9	XClk+	22	XClk-
10	X2+	23	X2-
11	X1+	24	X1-
12	X0+	25	X0-
13	Inner Shield	26	Inner Shield

Adapter cable ***AS-CBL-CL-ADPx-A-M2*** can be used to provide a standard Camera Link socket on the system case if the PC/104 stack does not allow the ***Phoenix-Dig24CL*** connector to line up with the case. This comprises a low profile right angle plug that plugs into ***Phoenix-Dig24CL***, 0.2m of special ribbon cable, and a panel mount Camera Link socket. The 'x' in the part number can be 'U' or 'D'. 'U' means that the ribbon cable exits upwards from ***Phoenix-Dig24CL***, 'D' exits downwards.

Detail of ***AS-CBL-CL-ADPU-B-M2***

I/O Connector

Phoenix-Dig24CL is fitted with a 50-way header for opto-isolated, RS-422 and TTL I/O.
Connector type: Standard 50 way 0.1" pitch right angle box header for use with IDC sockets.

PIN	SIGNAL	PIN	SIGNAL
1	OptoA1 Signal	2	OptoA1 GND
3	OptoA2 Signal	4	OptoA2 GND
5	AuxInA1+	6	AuxInA1-
7	AuxInA2+	8	AuxInA2-
9	GND	10	GND
11	OptoB1 Signal	12	OptoB1 GND
13	OptoB2 Signal	14	OptoB2 GND
15	AuxInB1+	16	AuxInB1-
17	AuxInB2+	18	AuxInB2-
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND
25	TTL A0 (*LSB*)	26	TTL A1
27	TTL A2	28	TTL A3
29	TTL A4	30	GND
31	TTL A5	32	TTL A6
33	TTL A7 (*MSB*)	34	TTL A Len
35	GND	36	CcOutA1 TTL
37	CcOutA2 TTL	38	TTL B0 (*LSB*)
39	TTL B1	40	TTL B2
41	TTL B3	42	TTL B4
43	GND	44	TTL B5
45	TTL B6	46	TTL B7 (*MSB*)
47	TTL B Len	48	GND
49	CcOutB1 TTL	50	CcOutB2 TTL

NOTES – Opto-Isolated and RS-422 I/O:

1. The opto-isolated I/O consists of a signal and a ground connection, all of which are all isolated from each other and the main GND signal.
2. The standard build of ***Phoenix-Dig24CL*** provides two opto-isolated inputs (OptoA1 & OptoB1) and two opto-isolated outputs (OptoA2 & OptoB2). These can be supplied with other combinations of input or output - please consult your distributor for more information.
3. The opto-isolated outputs are designed to sink up to 20mA of current from a 24V supply, and the inputs sense voltages between 3.3V and 24V as a logic high input.
4. AuxIn*XY* are RS-422 inputs used to connect external devices such as shaft encoders, or other trigger devices.

NOTES – TTL I/O:

1. The naming convention used is standard bit ordering, i.e. TTL A0 and TTL A7 are the LSB and MSB bits respectively of TTL Port A.
2. TTL *X* Len is a latch enable signal for the appropriate port. If it is held at a logical "0", then the current values on the I/O port pins are read. If it is held at a logical "1", then the values on the I/O port pins when TTL *X* Len transitioned from "0" to "1" are read. By default, this signal is fitted with a 4.7kΩ pulldown resistor, such that it can be left unconnected.
3. CcOutA*X* TTL are buffered output-only TTL versions of the CC*X* EIA-644 signals available on the Camera Link connector.

CONFORMANCE

PCI Interface:	PCI (Peripheral Component Interconnect) Bus to PCI Local Bus Specification Revision 2.2. The interface is 32-bit 33MHz supporting both 3.3V and 5V signalling. ***Phoenix-Dig24CL*** is Bus Master capable with 0 wait states, thus achieving burst rates of 133MBytes/sec, subject to host performance. The board is automatically mapped into memory space, requiring 16 MBytes of address range, and drives one interrupt output ("IntA", "IntB", "IntC" or "IntD" depending on the selected slot number).
PC/104-Plus:	***Phoenix-Dig24CL*** conforms to PC/104-Plus v1.2 which in turn is based on PC/104 v2.4.
Camera Link:	***Phoenix-Dig24CL*** conforms to v1.1 of the Camera Link specification.
Approvals:	EU CE mark for compliance with EMC EN 55022:1998 (class A) and EN 55024:1998 in accordance with EU directive 89/336/EEC. USA EMC FCC Class A. The printed circuit board is manufactured by UL recognised manufacturers and has a flammability rating of 94-V0.

PHYSICAL AND ENVIRONMENTAL DETAILS

Dimensions:	PCB: 96mm by 90mm Overall: 96mm by 101mm including connectors.
Approximate weight:	104g
Power consumption (typical):	+5V 700mA
Storage Temperature:	-40°C to +85°C.
Operating Temperature:	-40°C to +85°C.
Relative Humidity:	10% to 90% non-condensing (operating and storage).

ORDERING INFORMATION

PART NUMBER	*DESCRIPTION*
AS-PHX-D24CL-PC104P32-B	Camera Link frame grabber for Base Camera Link configuration. PCI bus with 32-bit, 33MHz, 3.3V/5V signalling. PC/104-Plus form factor.
AS-CBL-CL-MP-D-xM	Standard (MDR) to Standard (MDR) Camera Link cable *x* metres in length All cables are PoCL compliant. Standard stock lengths are 1m, 3m, 5m and 10m. Higher flex rating cables also available – contact your distributor for details.
AS-CBL-CL-ADPD-B-M2	Camera Link right angle adapter cable, exit down, 0.2m long.
AS-CBL-CL-ADPU-B-M2	Camera Link right angle adapter cable, exit up, 0.2m long.
AS-PHX-CBL-CH-FPC-M12	Chaining cable to connect two stacked ***Phoenix*** PC/104-Plus boards.
AS-PHX-SDK-xxx-CD	Software Development Kit for *xxx* operating system. For a full list of all supported operating systems please refer to the SDK datasheet, or contact your distributor.

An initial order for ***Phoenix*** with an SDK is supplied in a presentation case.

THE PHOENIX RANGE

The following products are available in the Phoenix range:

- CoaXPress frame grabbers.
- Base only Camera Link frame grabber.
- Base, Dual Base and Medium Camera Link frame grabber.
- Base, Medium and Full Camera Link frame grabber.
- 36-bit LVDS frame grabber.

They are available in standard PCI Express, PCI, PMC, CompactPCI, PCI/104-Express and PC/104-Plus form factors.

More products are in development. Please consult your distributor for information on the availability of other camera interface, PCI interface, and form factor options.

Active Silicon
COMPUTER IMAGING PRODUCTS
A SOLID STATE PLC GROUP COMPANY

CONTACT DETAILS

Europe & APAC:

Active Silicon Ltd
Pinewood Mews, Bond Close, Iver,
Bucks, SL0 0NA, UK.

Tel: +44 (0)1753 650600
Fax: +44 (0)1753 651661
Email info@activesilicon.com
Website: www.activesilicon.com

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Pyramid Imaging

945 East 11th Avenue Tampa, FL 33605
Phone: (813) 984-0125
Contact: Sales@ pyramidimaging.com
https://pyramidimaging.com