945 East 11th Avenue Tampa, FL 33605
Phone: (813) 984-0125
Contact: Sales@ pyramidimaging.com
https://pyramidimaging.com

Pyramid Imaging

TELEDYNE DALSA
Everywhereyoulook™

Teledyne DALSA • 7075 Place Robert-Joncas, Suite 142 • St-Laurent, Quebec, H4M 2Z2 • Canada
www.teledynedalsa.com

X64 Xcelera-CL LX1™

User's Manual

Edition 1.04

Part number OC-X1CM-LUSR1

NOTICE

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About Teledyne DALSA
Teledyne DALSA is an international high performance semiconductor and electronics company that designs, develops, manufactures, and markets digital imaging products and solutions, in addition to providing wafer foundry services.
Teledyne DALSA Digital Imaging offers the widest range of machine vision components in the world. From industry-leading image sensors through powerful and sophisticated cameras, frame grabbers, vision processors and software to easy-to-use vision appliances and custom vision modules.

Contents

Overview

X64 Xcelera-CL LX1 Part Numbers

X64 Xcelera-CL LX1 Board

Item	Product Number
X64 Xcelera-CL LX1 Base	OR-X1C0-XLB00
For OEM clients, this manual in printed form, is available on request	OC-X1CM-LUSR0

X64 Xcelera-CL LX1 Software

Item	Product Number
Sapera LT version 6.20 or later (required but sold separately) 1. Sapera LT: Provides everything you will need to build your imaging application 2. Current Sapera compliant board hardware drivers 3. Board and Sapera documentation (compiled HTML help, and Adobe Acrobat® (PDF) formats)	OC-SL00-0000000
(optional) Sapera Processing Imaging Development Library includes over 600 optimized image processing routines.	Contact Sales at Teledyne DALSA

X64 Xcelera-CL LX1 Cables & Accessories

Item	Product Number
(optional) Power interface cable required when supplying power to cameras	OR-COMC-POW03
(optional) Camera Link Video Input Cable: 1 meter 2 meter	 OC-COMC-CLNK0 OC-COMC-CLNK6
(optional) Power Over Camera Link (PoCL) Video Input Cable 2 meter SDR to MDR	OR-COMC-POCLD2
(optional) Power cable (connects +12V & GND from J10 to a 12 pin Hirose) see	OR-X1CC-XPOW1

About the X64 Xcelera-CL LX1 Frame Grabber

Series Key Features

- Monochrome or RGB Camera Link
- Horizontal & Vertical Flip supported on board
- RoHS compliant
- Supports Power Over Camera Link (PoCL)

See “Technical Specifications” on page 61 for detailed information.

User Programmable Configurations

Use the X64 Xcelera-CL LX1 firmware loader function in the Teledyne DALSA Device manager utility to select firmware for one of the supported modes. Firmware selection is made either during driver installation or manually later on (see "Firmware Update: Manual Mode" on page 11).

Currently there is one firmware choice:

- **Base Camera Link Input** (*installation default selection*)
  Support for one Base Camera Link port.

ACUPlus: Acquisition Control Unit

ACUPlus consists of a grab controller, one pixel packer, and one time base generator. ACUPlus delivers a flexible acquisition front end plus it supports pixel clock rates of up to 85MHz.

ACUPlus acquires variable frame sizes up to 256KB per horizontal line and up to 16 million lines per frame. ACUPlus can also capture an infinite number of lines from a linescan camera without losing a single line of data.

ACUPlus supports standard Camera Link multi-tap configurations from 8 to 24-bit/pixels.

DTE: Intelligent Data Transfer Engine

The X64 Xcelera-CL LX1 intelligent Data Transfer Engine ensures fast image data transfers between the board and the host computer with zero CPU usage. The DTE provides a high degree of data integrity during continuous image acquisition in a non-real time operating system like Windows. DTE consists of multiple independent DMA units, Tap Descriptor Tables, and Auto-loading Scatter-Gather tables.

PCI Express x1 Interface

The X64 Xcelera-CL LX1 is a universal PCI Express x1 board, compliant with the PCI Express 1.1 specification. The X64 Xcelera-CL LX1 board achieves transfer rates up to 185 Mbytes/sec. with all taps used when connected to a corresponding camera or sensor.

The X64 Xcelera-CL LX1 board occupies one PCI Express x1 expansion slot.

Important:

- Older computers may not support the maximum data transfer bandwidth defined for PCI Express x1.
- The X64 Xcelera-CL LX1 board can also be used in a PCI Express x4 or x8 slot typically without issue.
- If the computer only has a PCI Express x16 slot, the X64 Xcelera-CL LX1 may not be supported. Many computer motherboards only support x16 products in x16 slots (commonly used with graphic video boards). Full tests with the PC are required.

Advanced Controls Overview

Visual Indicators

X64 Xcelera-CL LX1 features a LED indicator to facilitate system installation and setup. This provides visual feedback indicating when the camera is connected properly and sending data.

External Event Synchronization

Trigger inputs and strobe signals are provided to precisely synchronize image captures with external events.

Camera Link Communications Ports

One PC independent communication port provide Camera Link controls for camera configurations. This port does not require additional PC resources like free interrupts or I/O address space. Accessible via the board device driver, the communication port presents a seamless interface to Windows-based standard communication applications like HyperTerminal, etc. The communication port is accessible directly from the Camera Link connector.

Quadrature Shaft Encoder

An important feature for web scanning applications, the Quadrature-Shaft-Encoder inputs allow synchronized line captures from external web encoders.

Development Software Overview

Sapera++ LT Library

Sapera++ LT is a powerful development library for image acquisition and control. Sapera++ LT provides a single API across all current and future TELEDYNE DALSA hardware. Sapera++ LT delivers a comprehensive feature set including program portability, versatile camera controls, flexible display functionality and management, plus easy to use application development wizards.

Sapera++ LT comes bundled with CamExpert, an easy to use camera configuration utility to create new, or modify existing camera configuration files.

Sapera Processing Library

Sapera Processing is a comprehensive set of C++ classes for image processing and analysis. Sapera Processing offers highly optimized tools for image processing, blob analysis, search (pattern recognition), OCR and barcode decoding.

Installing X64 Xcelera-CL LX1

Warning! (Grounding Instructions)

Static electricity can damage electronic components. Please discharge any static electrical charge by touching a grounded surface, such as the metal computer chassis, before performing any hardware installation.

If you do not feel comfortable performing the installation, please consult a qualified computer technician.

Important: Never remove or install any hardware component with the computer power on. Disconnect the power cord from the computer to disable the power standby mode. This prevents the case where some computers unexpectedly power up when a board is installed.

Sapera LT Library Installation

Note: to install Sapera LT and the X64 Xcelera-CL LX1 device driver, logon to the workstation as administrator or with an account that has administrator privileges.

The Sapera LT Development Library (or 'runtime library' if application execution without development is preferred) must be installed before the X64 Xcelera-CL LX1 device driver.

- Insert the TELEDYNE DALSA Sapera CD-ROM. If **AUTORUN** is enabled on your computer, the installation menu is presented.
- If **AUTORUN** is not enabled, use Windows Explorer and browse to the root directory of the CD-ROM. Execute **launch.exe** to start the installation menu and install the required Sapera components.
- The installation program will prompt you to reboot the computer.

Refer to *Sapera LT User's Manual* for additional details about Sapera LT.

Installing X64 Xcelera-CL LX1 Hardware and Driver

In a Windows XP/Vista/7 System

- Turn the computer off, disconnect the power cord (disables power standby mode), and open the computer chassis to allow access to the expansion slot area.
- Install the X64 Xcelera-CL LX1 into a free PCI Express x1 expansion slot. The X64 Xcelera-CL LX1 could also be installed in a PCI Express x4 or x8. Note that some computer's x16 slot may support the X64 Xcelera-CL LX1. The user needs to test each computer to verify support of an x1 product.
- Close the computer chassis and turn the computer on. Driver installation requires administrator rights for the current user of the computer.
- Windows will find the X64 Xcelera-CL LX1 and start its **Found New Hardware Wizard**. Click on the **Cancel** button to close the Wizard.
- Insert the TELEDYNE DALSA Sapera CD-ROM. If **AUTORUN** is enabled on your computer, the installation menu is presented. Install the X64 Xcelera-CL LX1 driver.
- If **AUTORUN** is not enabled, use Windows Explorer and browse to the root directory of the CD-ROM. Execute **launch.exe** to start the installation menu and install the X64 Xcelera-CL LX1 driver. During the late stages of the installation, the X64 Xcelera-CL LX1 firmware loader application starts. This is described in detail in the following section.
- If Windows displays any unexpected message concerning the installed board, power off the system and verify the X64 Xcelera-CL LX1 is installed in the slot properly.
- When using **Windows XP**, if a message stating that the X64 Xcelera-CL LX1 software has not passed **Windows Logo testing** is displayed, click on **Continue Anyway** to finish the X64 Xcelera-CL LX1 driver installation. Reboot the computer if prompted to do so.
- When using **Windows Vista/7**, a message asking to install the TELEDYNE DALSA device software is displayed. Click **Install**.

X64 Xcelera-CL LX1 Firmware Loader

The Device Manager-Firmware Loader program automatically executes at the end of the driver installation and on every subsequent reboot of the computer. It will determine if the X64 Xcelera-CL LX1 requires a firmware update. If firmware is required, a dialog displays and it also allows the user to load firmware for alternate operational modes of the X64 Xcelera-CL LX1.

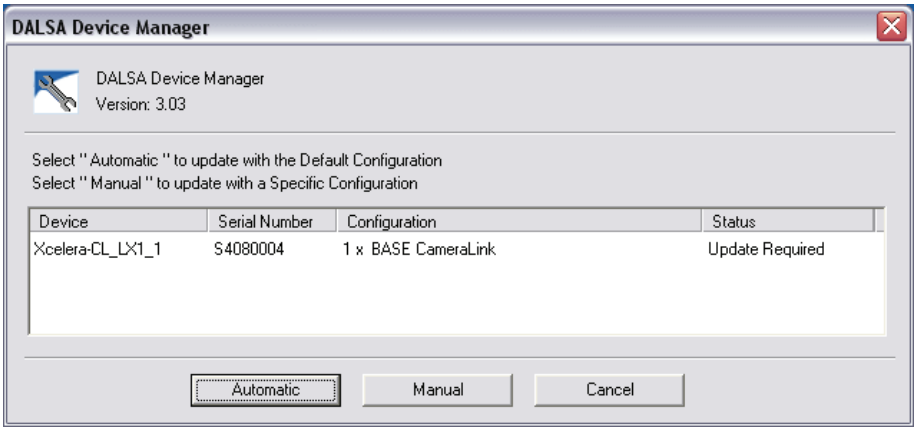
***Important*:** In the very rare case of firmware loader errors please see "Recovering from a Firmware Update Error" on page 25.

Firmware Update: Automatic Mode

Click **Automatic** to update the X64 Xcelera-CL LX1 firmware. The **X64 Xcelera-CL LX1** supports one firmware configuration for a Base camera.

See “Series Key Features” on page 6 and “User Programmable Configurations” on page 6 for details on all supported modes, which can be selected via a manual firmware update.

If there are multiple X64 Xcelera-CL LX1 boards in the system, they will all be updated with the new firmware. If any installed X64 Xcelera-CL LX1 board installed in a system already has the correct firmware version, an update is not required. In the following screen shot, a single X64 Xcelera-CL LX1 board is installed in the system and the default configuration is ready to be programmed.



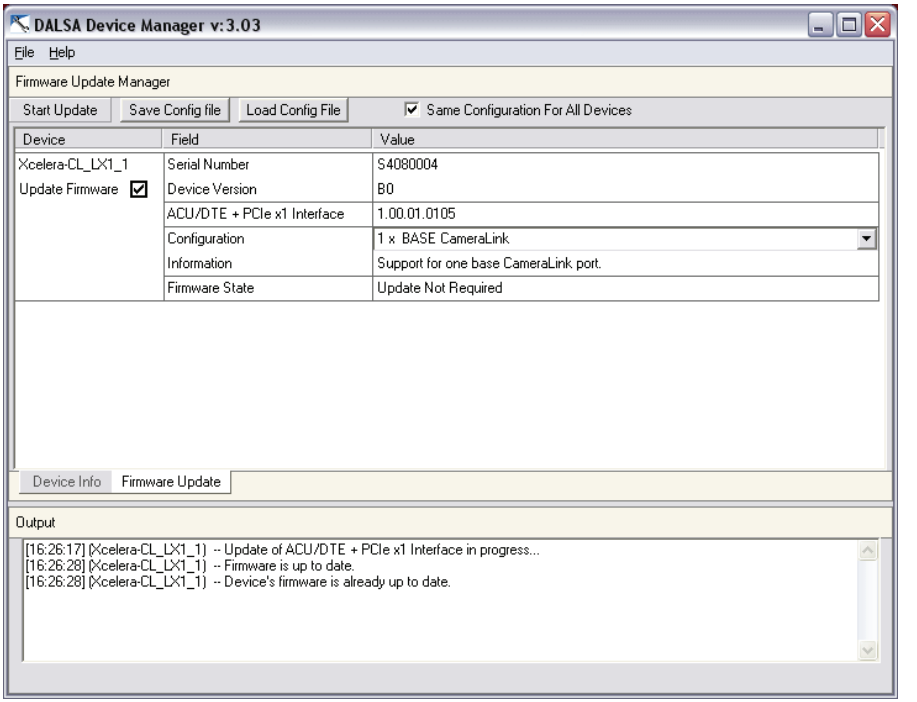
Firmware Update: Manual Mode

Click **Manual** mode to load firmware other then the default version or when, in the case of multiple X64 Xcelera-CL LX1 boards in the same system, each requires different firmware.

The figure below shows the Device Manager manual firmware screen. Information on all installed X64 Xcelera-CL LX1 boards, their serial numbers, and their firmware components are shown.

A manual firmware update is made as follows:

- Select the X64 Xcelera-CL LX1 to update via the board selection box (if there are multiple boards in the system)
- From the Configuration field drop menu select the firmware configuration required
- Click on the Start Update button
- Observe the firmware update progress in the message output window
- Close the Device manager program when the device reset complete message is shown.



Executing the Firmware Loader from the Start Menu

If required, the X64 Xcelera-CL LX1 Firmware Loader program can be executed via the Windows Start Menu shortcut **Start • Programs • Teledyne DALSA • X64 Xcelera-CL LX1 Driver • Firmware Update**. A firmware change after installation would be required to select a different configuration mode. See "User Programmable Configurations" on page 6.

Upgrading Sapera or any Board Driver

When installing a new version of Sapera or a Teledyne DALSA acquisition board driver in a computer with a previous installation, the current version **must** be un-installed first. Upgrade scenarios are described below.

Board Driver Upgrade Only

Minor upgrades to acquisition board drivers are typically distributed as ZIP files available in the Teledyne DALSA web site. Board driver revisions are also available on the next release of the Sapera CD-ROM.

Often minor board driver upgrades do not require a new revision of Sapera. To confirm that the current Sapera version will work with the new board driver:

- Check the new board driver ReadMe file before installing, for information on the minimum Sapera version required.
- If the ReadMe file does not specify the Sapera version, contact Teledyne DALSA Technical Support (see "Technical Support" on page 82).

To upgrade the board driver only:

- Logon the computer as an administrator or with an account that has administrator privileges.
- In Windows XP, from the start menu select **Start • Control Panel • Add or Remove Programs**. Select the Xcelera board driver and click **Remove**.
- Windows XP only:
    - When the driver un-install is complete, reboot the computer.
    - Logon the computer as an administrator again.
- In Windows Vista/7, from the start menu select **Start • Control Panel • Programs and Features**. Double-click the Xcelera board driver and click **Remove**.
- Install the new board driver. Run **Setup.exe** if installing manually from a downloaded driver file.
- If the new driver is on a Sapera CD-ROM follow the installation procedure described in "Installing X64 Xcelera-CL LX1 Hardware and Driver" on page 10.
- Note that you can not install a board driver without Sapera LT installed on the computer.

Sapera and Board Driver Upgrades

When both Sapera and the acquisition board driver are upgraded, follow the procedure described below.

- Logon the computer as an administrator or with an account that has administrator privileges.
- In Windows XP, from the start menu select **Start • Control Panel • Add or Remove Programs**. Select the Xcelera board driver and click **Remove**. Follow by also removing the older version of Sapera LT.
- In Windows Vista/7, from the start menu select **Start • Control Panel • Programs and Features**. Double-click the Xcelera board driver and click **Remove**. Follow by also removing the older version of Sapera LT.
- Reboot the computer and logon the computer as an administrator again.
- Install the new versions of Sapera and the board driver as if this was a first time installation. See "Sapera LT Library Installation" on page 9 and "Installing X64 Xcelera-CL LX1 Hardware and Driver" on page 10 for installation procedures.

Enabling the Camera Link Serial Control Port

The Camera Link cabling specification includes a serial communication port for direct camera control by the frame grabber (see "J1: MDR 26-Pin Female Camera Link Connector " on page 67). The X64 Xcelera-CL LX1 driver supports this serial communication port either directly or by mapping it to a host computer COM port. Any serial port communication program, such as Windows HyperTerminal, can connect to the camera in use and modify its function modes via its serial port controls. The X64 Xcelera-CL LX1 serial port supports communication speeds from 9600 to 115200 bps.

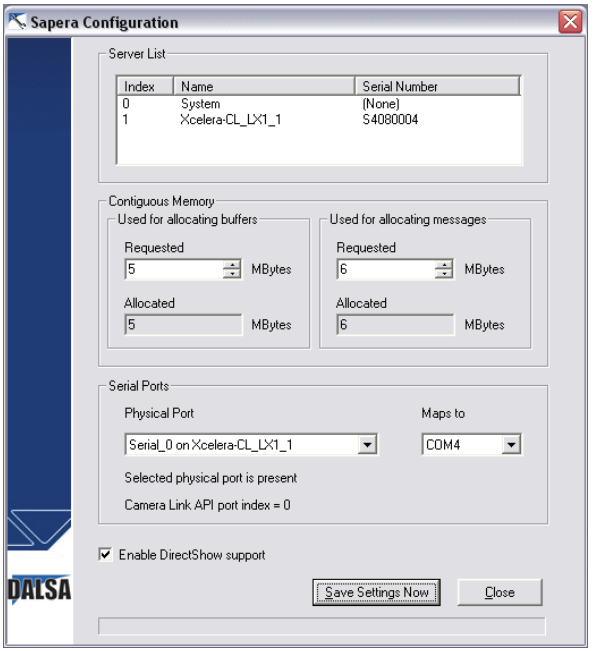
Note: if your serial communication program can directly select the X64 Xcelera-CL LX1 serial port then mapping to a system COM port is not necessary.

The X64 Xcelera-CL LX1 serial port can be mapped to an available COM port by using the Sapera Configuration tool. Run the program from the Windows start menu: **Start • Programs • Teledyne DALSA • Sapera LT • Sapera Configuration**.

COM Port Assignment

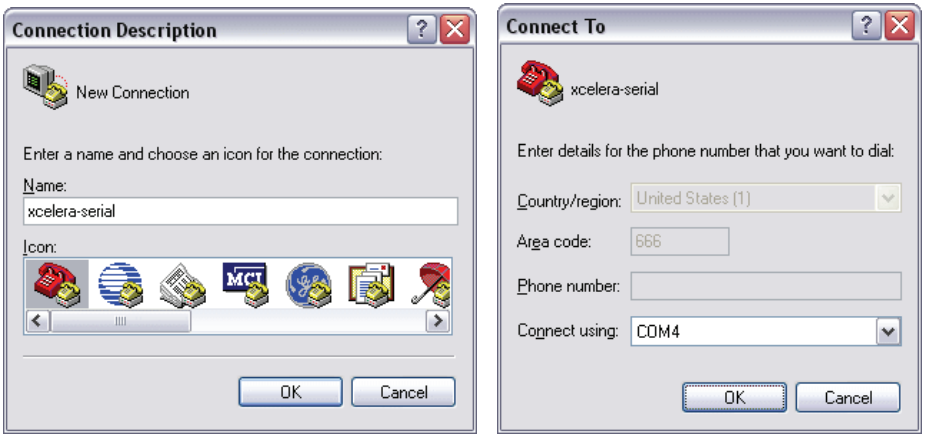
The lower section of the Sapera Configuration program screen contains the serial port configuration menu. Configure as follows:

- Use the **Physical Port** drop menu to select the Sapera board device from all available Sapera boards with serial ports (when more then one board is in the system).
- Use the **Maps to** drop menu to assign an available COM number to that Sapera board's serial port.
- Click on the **Save Settings Now** button then the **Close** button. You are prompted to reboot your computer to enable the serial port mapping.
- The X64 Xcelera-CL LX1 serial port, now mapped to COM4 in this example, is available as a serial port to any serial port application for camera control. Note that this serial port is not listed in the **Windows Control Panel•System Properties•Device Manager** because it is a logical serial port mapping.
- An example setup using Windows HyperTerminal follows.

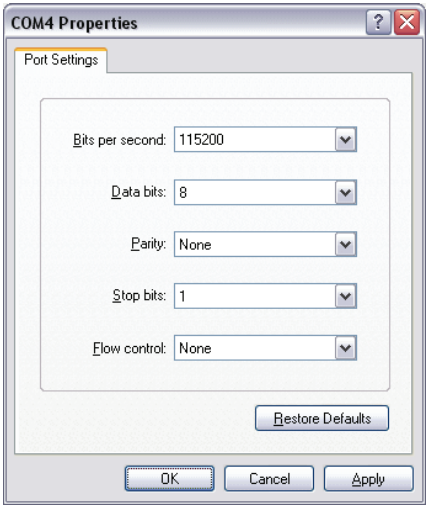


Setup Example with Windows HyperTerminal

- Run HyperTerminal and type a name for the new connection when prompted. Then click OK.
- On the following dialog screen select the port associated with the X64 Xcelera-CL LX1.



HyperTerminal now presents a dialog to configure the COM port properties. Change settings as required by the camera you are connecting to. Note that the X64 Xcelera-CL LX1 serial port does not support hardware flow control.



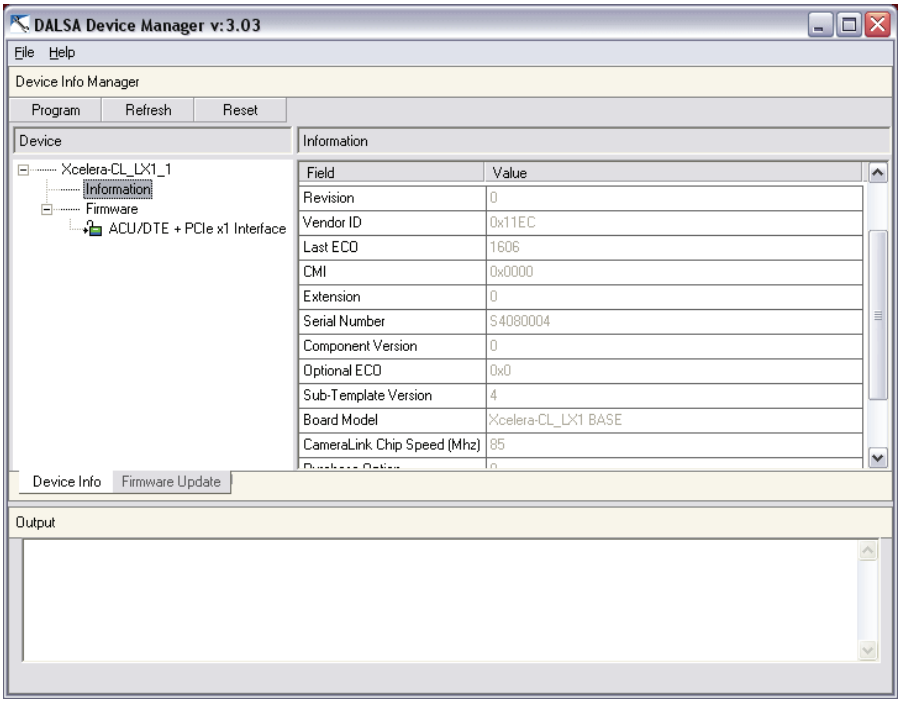
Displaying X64 Xcelera-CL LX1 Board Information

The Device Manager program also displays information about the X64 Xcelera-CL LX1 boards installed in the system. To view board information run the program via the Windows Start Menu shortcut **Start • Programs • Teledyne DALSA • X64 Xcelera-CL LX1 Device Driver • DeviceManager**.

Device Manager – Board Viewer

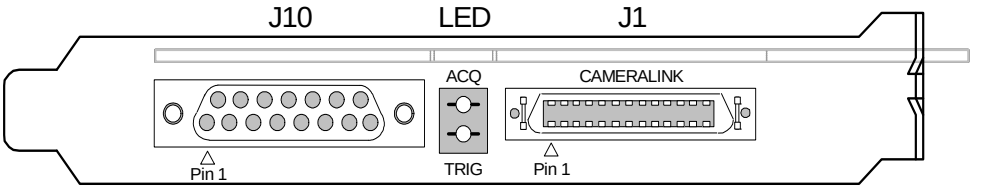
The following screen image shows the Device Manager program with the Information/Firmware tab active. The left window displays all X64 Xcelera-CL LX1 boards in the system and their individual device components. The right window displays the information stored in the selected board device. This example screen shows the X64 Xcelera-CL LX1 information contained in the EEProm component.

The X64 Xcelera-CL LX1 device manager report file (BoardInfo.txt) is generated by clicking **File • Save Device Info**. This report file may be requested by Teledyne DALSA Technical Support to aid in troubleshooting installation or operational problems.



Camera to Camera Link Connections

X64 Xcelera-CL LX1 End Bracket



Connector Bracket

The hardware installation process is completed with the connection of a supported camera to the X64 Xcelera-CL LX1 board using Camera Link cable (see “Camera Link Cables” on page 79).

- The X64 Xcelera-CL LX1 board supports a camera with one Camera Link MDR-26 connector (one Base– see “Data Port Summary” on page 78 for information on Camera Link configurations).
- Connect the camera to the Camera Link connector with a Camera Link cable.

Refer to section "Connector and Switch Specifications" on page 65 for details on the Camera Link connectors.

Note: If the camera is powered by the X64 Xcelera-CL LX1, refer to "Connector, Switch, Jumper Description List" on page **65** for power connections.

Contact Teledyne DALSA or browse our web site for the latest information on X64 Xcelera-CL LX1 supported cameras.

Configuring Sapera

Viewing Installed Sapera Servers

The Sapera configuration program (**Start • Programs • Teledyne DALSA • Sapera LT • Sapera Configuration**) allows the user to see all available Sapera servers for the installed Sapera-compatible boards. The **System** entry represents the system server. It corresponds to the host machine (your computer) and is the only server that should always be present.

Increasing Contiguous Memory for Sapera Resources

The **Contiguous Memory** section lets the user specify the total amount of contiguous memory (a block of physical memory, occupying consecutive addresses) reserved for the resources needed for **Sapera buffers** allocation and **Sapera messaging**. For both items, the **Requested** value dialog box shows the driver default memory setting while the **Allocated** value displays the amount of contiguous memory that has been allocated successfully. The default values will generally satisfy the needs of most applications.

The **Sapera buffers** value determines the total amount of contiguous memory reserved at boot time for the allocation of dynamic resources used for host frame buffer management such as DMA descriptor tables plus other kernel needs. Adjust this value higher if your application generates any out-of-memory error while allocating host frame buffers. You can approximate the amount of contiguous memory required as follows:

- Calculate the total amount of host memory used for frame buffers
  [number of frame buffers • number of pixels per line • number of lines • (2 - if buffer is 10 or 12 bits)].
- Provide 1MB for every 256 MB of host frame buffer memory required.
- Add an additional 1 MB if the frame buffers have a short line length, say 1k or less
  (the increased number of individual frame buffers requires more resources).
- Add an additional 2 MB for various static and dynamic Sapera resources.
- Test for any memory error when allocating host buffers. Simply use the Buffer menu of the Sapera Grab demo program (see "Grab Demo Overview" on page 37) to allocate the number of host buffers required for your acquisition source. Feel free to test the maximum limit of host buffers possible on your host system – the Sapera Grab demo will not crash when the requested number of host frame buffers cannot be allocated.

Host Computer Frame Buffer Memory Limitations

When planning a Sapera application and its host frame buffers used, plus other Sapera memory resources, do not forget the Windows operating system memory needs. Window XP as an example, should always have a minimum of 128 MB for itself.

A Sapera application using *scatter gather buffers* could consume most of the remaining system memory. When using frame buffers allocated as a *single contiguous memory block*, typical limitations are one third of the total system memory with a maximum limit of approximately 100 MB. See the Buffer menu of the Sapera Grab demo program for information on selecting the type of host buffer memory allocation.

Contiguous Memory for Sapera Messaging

The current value for **Sapera messaging** determines the total amount of contiguous memory reserved at boot time for messages allocation. This memory space is used to store arguments when a Sapera function is called. Increase this value if you are using functions with large arguments, such as arrays and experience any memory errors.

Troubleshooting Installation Problems

Overview

The X64 Xcelera-CL LX1 (and the X64 family of products) has been tested by Teledyne DALSA in a variety of computers. Although unlikely, installation problems may occur due to the constant changing nature of computer equipment and operating systems. This section describes what the user can verify to determine the problem or the checks to make before contacting Technical Support.

If you require help and need to contact Technical Support, make detailed notes on your installation and/or test results for our technical support to review. See "Technical Support" on page 82 for contact information.

Problem Type Summary

X64 Xcelera-CL LX1 problems are either installation types where the board hardware is not recognized on the PCIe bus (i.e. trained) or function errors due to camera connections or bandwidth issues. The following links jump to various topics in this troubleshooting section.

First Step: Check the Status LED

A RED Status LED 1 indicates a camera problem, while various Green states indicate the acquisition mode.

Status LED 2, if flashing RED, indicates a PCIe bus problem. If you run the PCI Diagnostics tool, the LX1 is not in the PCI device list. If the board is installed in a computer which supports PCIe GEN2 expansion slots, see section "J8: GEN2 Slot (PCIe generation 2) Workaround" on page 75.

The complete status LED description is available in the technical reference section (see "Status LEDs Functional Description" on page 66).

Possible Installation Problems

- **Hardware PCI bus conflict:** When a new installation produces PCI bus error messages or the board driver doesn't install, it is important to verify that there are no conflicts with other PCI or system devices already installed. Use the Teledyne DALSA PCI Diagnostic tool as described in "Checking for PCI Bus Conflicts" on page 23. Also verify the installation via the "Driver Information via the Device Manager Program" on page 26.
- **Gen2 slot errors:** There is a PCI bus error message from the computer bios. Follow the instructions "GEN2 PCI Slot Computer Issue" on page 25.
- **Verify Sapera and Board drivers:** If there are errors when running applications, confirm that all Sapera and board drivers are running. See "Sapera and Hardware Windows Drivers" on page 25 for details. In addition, Teledyne DALSA technical support will ask for the log file of messages by Teledyne DALSA drivers. Follow the instructions describe in "Log Viewer" on page 28.
- **Firmware update error:** There was an error during the board firmware update procedure. This usually is easily corrected by the user. Follow the instructions "Recovering from a Firmware Update Error" on page 25.
- Installation went well but the board doesn't work or stopped working. Review theses steps described in "Symptoms: CamExpert Detects no Boards" on page 28.

Possible Functional Problems

- **Driver Information:** Use the Teledyne DALSA device manager program to view information about the installed X64 Xcelera-CL LX1 board and driver. See "Driver Information via the Device Manager Program" on page 26.

Sometimes the problem symptoms are not the result of an installation issue but due to other system issues. Review the sections described below for solutions to various X64 Xcelera-CL LX1 functional problems.

- "Symptom: X64 Xcelera-CL LX1 Does Not Grab" on page 28
- "Symptom: Card grabs black" on page 29
- "Symptom: Card acquisition bandwidth is less than expected" on page 29

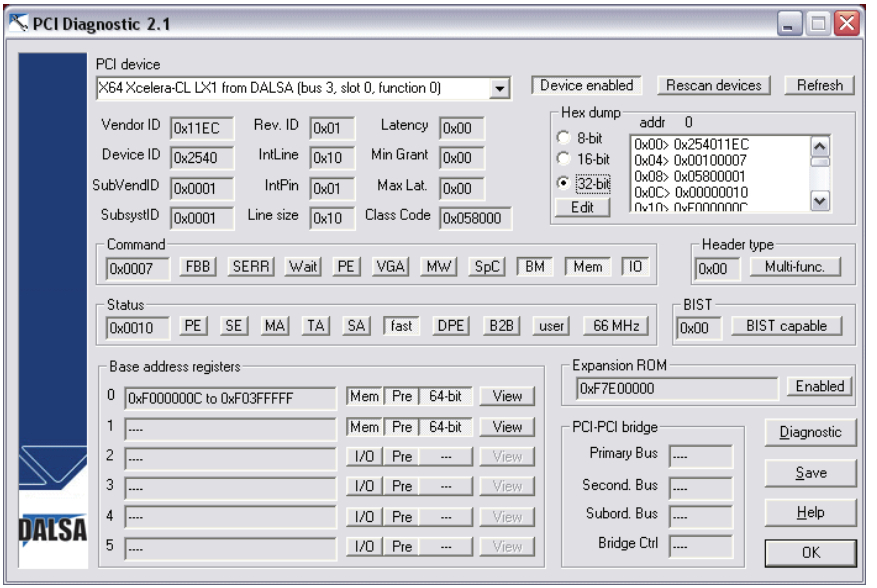
Troubleshooting Procedures

The following sections provide information and solutions to possible X64 Xcelera-CL LX1 installation and functional problems. These topics are summarized in the previous section of this manual.

Checking for PCI Bus Conflicts

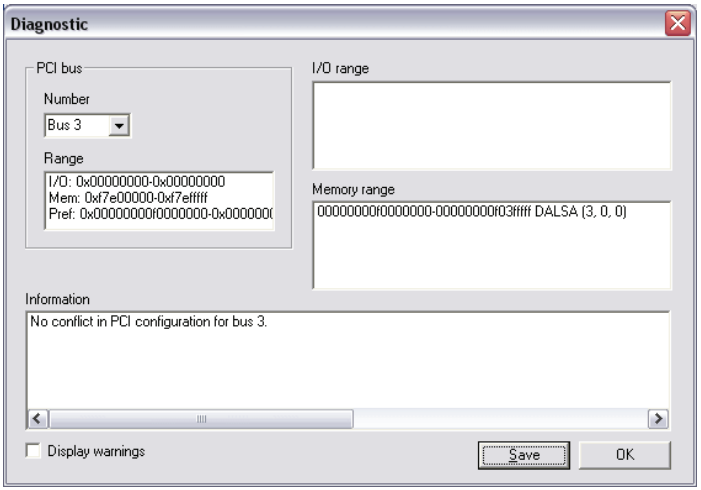
One of the first items to check when there is a problem with any PCI board is to examine the system PCI configuration and ensure that there are no conflicts with other PCI or system devices. The *PCI Diagnostic* program (**cpcidiag.exe**) allows examination of the PCI configuration registers and can save this information to a text file. Run the program via the Windows Start Menu shortcut **Start • Programs • Teledyne DALSA • Sapera LT • Tools • PCI Diagnostics**.

As shown in the following screen image, use the first drop menu to select the PCI device to examine. Select the device from Teledyne DALSA. Note the bus and slot number of the installed board (this will be unique for each system unless systems are setup identically). Click on the **Diagnostic** button to view an analysis of the system PCI configuration space.



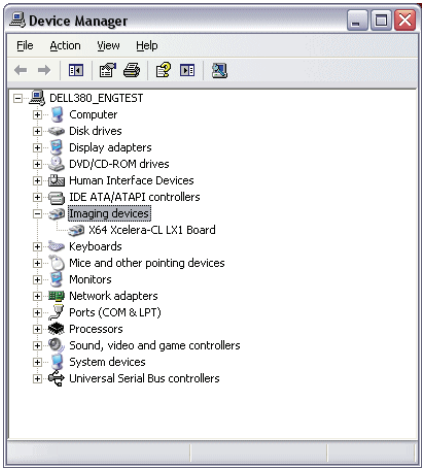
Clicking on the **Diagnostic** button opens a new window with the diagnostic report. From the PCI Bus Number drop menu select the bus number that the X64 Xcelera-CL LX1 is installed in—in this example the slot is bus 3.

The window now shows the I/O and memory ranges used by each device on the selected PCI bus. The information display box will detail any PCI conflicts. If there is a problem, click on the **Save** button. A file named '**pcidiag.txt'** is created (in the Sapera\bin directory) with a dump of the PCI configuration registers. Email this file when requested by the Technical Support group along with a full description of your computer.



Windows Device Manager

In Windows use the Start Menu shortcut **Start • Settings • Control Panel • System • Hardware • Device Manager**. As shown in the following screen images, look for *X64 Xcelera-CL LX1* board under "Imaging Devices". Double-click and look at the device status. You should see "This device is working properly." Go to "Resources" tab and make certain that the device is mapped and has an interrupt assigned to it, without any conflicts.



GEN2 PCI Slot Computer Issue

At boot time, the LX1 status LED 2 keeps on flashing red. If you run the PCI Diagnostics tool, the LX1 is not in the PCI device list. If the board is installed in a computer which supports PCIe GEN2 expansion slots, see section "J8: GEN2 Slot (PCIe generation 2) Workaround" on page 75.

Sapera and Hardware Windows Drivers

The next step is to make certain the appropriate drivers have started successfully during the boot sequence. Example, click on the **Start • Programs • Accessories • System Tools • System Information • Software Environment**. Click on **System Drivers**. Make certain the following drivers have started for the **X64 Xcelera-CL LX1**.

Device	Description	Type	Started
CorX64XceleraLx1	X64 Xcelera-CL LX1 driver	Kernel Driver	Yes
CorLog	Sapera Log viewer	Kernel Driver	Yes
CorMem	Sapera Memory manager	Kernel Driver	Yes
CorPci	Sapera PCI configuration	Kernel Driver	Yes
CorSerial	Sapera Serial Port manager	Kernel Driver	Yes

Technical Support may request that you check the status of these drivers as part of the troubleshooting process.

Recovering from a Firmware Update Error

This procedure is required if any failure occurred while updating the X64 Xcelera-CL LX1 firmware on installation or during a manual firmware upgrade. On the rare occasion the board has corrupted firmware, any Sapera application such as CamExpert or the grab demo program will not find an installed board to control.

Possible reasons for firmware loading errors or corruption are:

- Computer system mains power failure or deep brown-out.
- PCI bus or checksum errors.
- PCI bus timeout conditions due to other devices.
- User forcing a partial firmware upload using an invalid firmware source file.

When the X64 Xcelera-CL LX1 firmware is corrupted, executing a manual firmware upload will not work because the firmware loader can not communicate with the board. In an extreme case, corrupted firmware may even prevent Windows from booting.

***Solution*:** The user manually forces the board to initialize from write protected firmware designed only to allow driver firmware uploads. When the firmware upload is complete, the board is then rebooted to initialize in its normal operational mode.

- Note that this procedure may require removing the X64 Xcelera-CL LX1 board several times from the computer.
- ***Important*:** The Boot Recovery Mode jumper for the X64 Xcelera-CL LX1 is J8 pin 15& 16 (see "J8: Normal or Safe Boot Select Jumper" on page 75). In the connectors and jumpers reference section, identify the jumper location.
- Shut down Windows and power OFF the computer.
- Remove the shorting jumper from J8 pin 15& 16 for the boot recovery mode position (safe boot). (The default position is shorting jumper installed on J8 pin 15&16 for normal operation).
- Power on the computer. Windows will boot normally.
- When Windows has started, do a manual firmware update procedure to update the firmware again (see "Executing the Firmware Loader from the Start Menu" on page 12).
- When the update is complete, shut down Windows and power off the computer.
- Install the shorting jumper back on J8 pin 15&16 (that is, default position) and power on the computer once again.
- Verify that the frame grabber is functioning by running a Sapera application such as CamExpert. The Sapera application will now be able to communicate with the X64 Xcelera-CL LX1 board.

Driver Information via the Device Manager Program

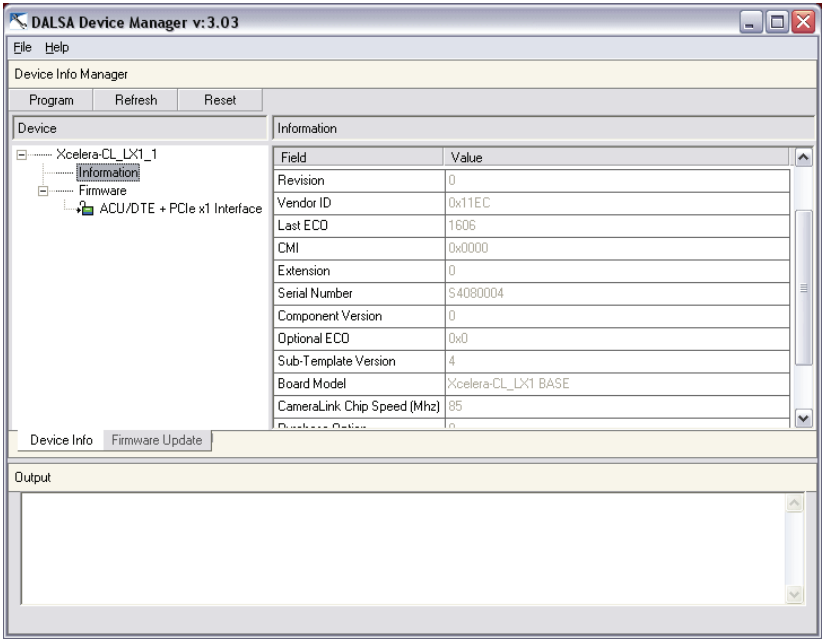
The Device Manager program provides a convenient method of collecting information about the installed X64 Xcelera-CL LX1. System information such as operating system, computer CPU, system memory, PCI configuration space, plus X64 Xcelera-CL LX1 firmware information can be displayed or written to a text file (default file name – BoardInfo.txt). Note that this is a second function mode of the same program used to manually upload firmware to the X64 Xcelera-CL LX1.

Execute the program via the Windows Start Menu shortcut **Start • Programs • Teledyne DALSA • X64 Xcelera-CL LX1 Device Driver • Device Manager**. If the Device Manager program does not run, it will exit with a message that the board was not found. Since the X64 Xcelera-CL LX1 board must have been in the system to install the board driver, possible reasons for an error are:

- Board was removed
- Board driver did not start or was terminated
- PCI conflict after some other device was installed

Information Window

The following figure shows the Device Manager information screen. Click to highlight one of the board components and the information for that item is shown on the right hand window, as described below.



- Select **Information** to display identification and information stored in the X64 Xcelera-CL LX1 firmware.
- Select **Firmware** to display version information for the firmware components.
- Select one of the firmware components to load *custom* firmware when supplied by Teledyne DALSA engineering for a future feature.
- Click on **File • Save Device Info** to save all information to a text file. Email this file when requested by Technical Support.

Log Viewer

The third step in the verification process is to save in a text file the information collected by the Log Viewer program. Run the program via the Windows Start Menu shortcut **Start • Programs • Teledyne DALSA • Sapera LT • Tools • Log Viewer**.

The Log Viewer lists information about the installed Teledyne DALSA drivers. Click on **File • Save** and you will be prompted for a text file name to save the Log Viewer contents. Email this text file to Technical Support when requested or as part of your initial contact email.

Symptoms: CamExpert Detects no Boards

- **If using Sapera version 6.00 or later:**
  When starting CamExpert, if no Teledyne DALSA board is detected, CamExpert will start in offline mode. There is no error message and CamExpert is functional for creating or modifying a camera configuration file. If CamExpert should have detected the installed board, troubleshoot the installation problem as described below.

Troubleshooting Procedure

When CamExpert detects no installed board, there could be a hardware problem, a PnP problem, a PCI problem, a kernel driver problem, or a software installation problem.

- Make certain that the card is properly seated in PCIe slot.
- Perform all installation checks described in this section before contacting Technical Support.
- Try the board in a different PCIe slot if available.

Symptom: X64 Xcelera-CL LX1 Does Not Grab

You are able to start Sapera CamExpert but you do not see an image and the frame rate displayed is 0.

- Verify power is connected to the camera.
- Verify the camera and timing parameters with the camera in free run mode.
- Verify you can grab with the camera in free run mode.
- Make certain that you provide an external trigger if the camera configuration file requires one. Use the software trigger feature of CamExpert if you do not have a trigger source.
- Make certain that the camera is properly connected to the cable.
- Make certain that the camera is configured for the proper mode of operation. This must match the camera configuration file. Refer to your camera datasheet.
- Try to snap one frame instead of continuous grab.
- Perform all installation checks described in this section before contacting Technical Support.

Symptom: Card grabs black

You are able to use Sapera CamExpert, the displayed frame rate is as expected, but the display is always black.

- Set your camera to manual exposure mode and set the exposure to a longer period, plus open the lens iris.
- Try to snap one frame instead of continuous grab.
- This problem is sometimes caused by a PCIe transfer issue. A PCIe transfer takes place, so the frame rate is above 0 but nevertheless no image is displayed in CamExpert.
- Make certain that BUS MASTER bit in the PCIe configuration space is activated. Look in PCI Diagnostics for **BM** button under "Command" group. Make certain that the **BM** button is activated.
- Perform all installation checks described in this section before contacting Technical Support.

Symptom: Card acquisition bandwidth is less than expected

The X64 Xcelera-CL LX1 acquisition bandwidth is less than expected.

- Review the system for problems or conflicts with other expansion boards or drivers.
- Remove other PCI Express, PCI-32 or PCI-64 boards and check acquisition bandwidth again. Engineering has seen cases where other PCI boards in some systems cause limitations in transfers. Each system, with its combination of system motherboard and PCI boards, will be unique and will need to be tested for bandwidth limitations affecting the imaging application.
- Is the X64 Xcelera-CL LX1 installed in a PCI Express x16 slot?
  Note that some computer's x16 slot may not support non x16 boards. Check the computer documentation.

CamExpert Quick Start

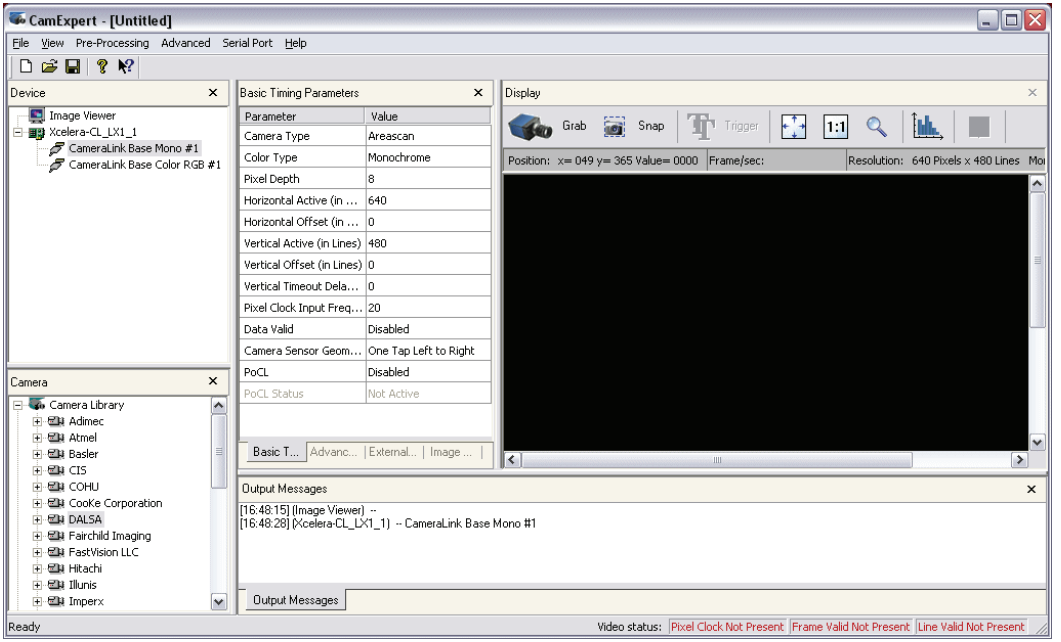
Interfacing Cameras with CamExpert

CamExpert is the camera interfacing tool for frame grabber boards supported by the Sapera library. CamExpert generates the Sapera camera configuration file (*yourcamera.ccf*) based on timing and control parameters entered. For backward compatibility with previous versions of Sapera, CamExpert also reads and writes the *.cca and *.cvi camera parameter files.

Every Sapera demo program starts by a dialog window to select a camera configuration file. Even when using the X64 Xcelera-CL LX1 with common video signals, a camera file is required. Therefore CamExpert is typically the first Sapera application run after an installation. Obviously existing .ccf files can be copied to the new installation when similar cameras are used.

CamExpert Example with a Monochrome Camera

The image below shows CamExpert with the X64 Xcelera-CL LX1. The camera outputs monochrome 8-bit video on a Camera Link interface. After selecting the camera model, the timing parameters are displayed and the user can test by clicking on *Grab*. Descriptions of the CamExpert windows follows the image.



The CamExpert sections are:

- **Device:** Select which acquisition device to control and configure a camera file for. Required in cases where there are multiple boards in a system and also when one board supports multiple acquisition types. Note in this example, the X64 Xcelera-CL LX1 was installed with firmware support for monochrome or RGB base cameras.
- **Camera:** Select the timing for a specific camera model included with the Sapera installation or a standard video standard. The *User's* subsection is where created camera files are stored.
- **Timing & Control Parameters:** The central section of CamExpert provides access to the various Sapera parameters supported by X64 Xcelera-CL LX1. There are four or five tabs dependent on the acquisition board, as described below:

Basic Timing Parameters	Basic parameters used to define the timing of the camera. This includes the vertical, horizontal, and pixel clock frequency. This tab is sufficient to configure a free-running camera.
Advanced Control Parameters	Advanced parameters used to configure camera control mode and strobe output. Also provides analog signal conditioning (brightness, contrast, DC restoration, etc.) for analog boards.
External Trigger Parameters	Parameters to configure the external trigger characteristics.
Image Buffer and AOI Parameters	Control of the host buffer dimension and format.
Multi-Camera Control Parameters	Dependent on the frame acquisition board, provides camera selection and color planar transfer selection.

- **Display:** An important component of CamExpert is its live acquisition display window which allows immediate verification of timing or control parameters without the need to run a separate acquisition program. **Grab** starts continuous acquisition (button then toggles to **Freeze** to stop). **Snap** is a single frame grab. **Trigger** is a software trigger to emulate an external source.
- **Output Messages and Bottom Status Bar:** Events and errors are logged for review. Camera connection status is displayed where green indicates signal present.

For context sensitive help click on the  button then click on a camera configuration parameter. A short description of the configuration parameter will be shown in a popup. Click on the  button to open the help file for more descriptive information on CamExpert.

CamExpert Demonstration and Test Tools

The CamExpert utility also includes a number of demonstration features which make CamExpert the primary tool to configure, test and calibrate your camera and imaging setup. Display tools include, image pixel value readout, image zoom, and line profiler.

Camera Types & Files Applicable to the X64 Xcelera-CL LX1

The X64 Xcelera-CL LX1 supports digital area scan or linescan cameras using the Camera Link interface standard. See "Camera to Camera Link Connections" on page 18 for information on connecting a Camera Link camera.

Contact Teledyne DALSA or browse our web site for the latest information and application notes on X64 Xcelera-CL LX1 supported cameras.

Camera Files Distributed with Sapera

The Sapera distribution CDROM includes camera files for a selection of X64 Xcelera-CL LX1 supported cameras. Using the Sapera CamExpert program, you may use the camera files (CCA) provided to generate a camera configuration file (CCF) that describes the desired camera and frame grabber configuration.

Teledyne DALSA continually updates a camera application library composed of application information and prepared camera files. Camera files are ASCII text and can be read with Windows Notepad on any computer without having Sapera installed.

Overview of Sapera Acquisition Parameter Files (*.ccf or *.cca/*.cvi)

Concepts and Differences between the Parameter Files

There are two components to the legacy Sapera acquisition parameter file set: CCA files (also called cam-files) and CVI files (also called VIC files, that is, video input conditioning). The files store video-signal parameters (CCA) and video conditioning parameters (CVI), which in turn simplifies programming the frame-grabber acquisition hardware for the camera in use. **Sapera LT 5.0** and later introduces a new camera configuration file (**CCF**) that combines the CCA and CVI files into one file.

Typically, a camera application will use a CCF file per camera operating mode (or one CCA file in conjunction with several CVI files, where each CVI file defines a specific camera operating mode). An application can also have multiple CCA/CCF files so as to support different image format modes supported by the camera or sensor (such as image binning or variable ROI).

CCF File Details

Files using the ".CCF" extension, (Camera Configuration files), are essentially the camera (CCA) and frame grabber (CVI) parameters grouped into one file for easier configuration file management. This is the default Camera Configuration file used with Sapera LT 5.0 and later and the CamExpert utility.

CCA File Details

Teledyne DALSA distributes camera files using the ".CCA" extension, (CAMERA files), which contain all parameters describing the camera video signal characteristics and operation modes (what the camera outputs). The Sapera parameter groups within the file are:

- Video format and pixel definition.
- Video resolution (pixel rate, pixels per line, lines per frame).
- Synchronization source and timing.
- Channels/Taps configuration.
- Supported camera modes and related parameters.
- External signal assignment.

CVI File Details

Legacy files using the ".CVI" extension contain all operating parameters related to the frame grabber board - what the frame grabber can actually do with camera controls or incoming video. The Sapera parameter groups within the file are:

- Activate and set any supported camera control mode or control variable.
- Define the integration mode and duration.
- Define the strobe output control.
- Allocate the frame grabber transfer ROI, the host video buffer size and buffer type (RGB8888, MONO8, MONO16).
- Configuration of line/frame trigger parameters such as source (internal via the frame grabber /external via some outside event), electrical format (TTL, RS-422, OPTO-isolated), and signal active edge or level characterization.

Camera Interfacing Check List

Before interfacing a camera from scratch with CamExpert:

- Confirm that Teledyne DALSA has not already published an application note with camera files included.
- Confirm that the correct version or board revision of X64 Xcelera-CL LX1 is used. Confirm that the required firmware is loaded into the X64 Xcelera-CL LX1.
- Confirm that Sapera does not already have a .cca file for your camera installed on your hard disk. If there is a .cca file supplied with Sapera, then use CamExpert to automatically generate the .ccf file with default parameter values matching the frame grabber capabilities.
- Check if the Sapera installation has a similar type of camera file. A similar .cca file can be loaded into CamExpert where it is modified to match timing and operating parameters for your camera, and lastly save them as Camera Configuration file (.ccf).
- Finally, if your camera type has never been interfaced, run CamExpert after installing Sapera and the acquisition board driver, select the board acquisition server, and manually enter the camera parameters.

Sapera Demo Applications

Grab Demo Overview

Program	**Start•Programs•Teledyne DALSA•Sapera LT•Demos•Frame Grabber•Grab Demo**
Program file	**…\Sapera\Demos\Classes\vc\GrabDemo\Release\GrabDemo.exe**
Workspace	**…\Sapera\Demos\Classes\vc\SapDemos.dsw**
.NET Solution	**…\Sapera\Demos\Classes\vc\SapDemos_2003.sln**
Description	This program demonstrates the basic acquisition functions included in the Sapera library. The program allows you to acquire images, either in continuous or in one-shot mode, while adjusting the acquisition parameters. The program code may be extracted for use within your own application.
Remarks	This demo is built using Microsoft Visual Studio .NET 2003 using the MFC library. It is based on Sapera C++ classes. See the Sapera User's and Reference manuals for more information.

Using the Grab Demo

Server Selection

Run the grab demo from the start menu **Start•Programs•Teledyne DALSA•Sapera LT•Demos•Frame Grabbers•Grab Demo**.

The demo program first displays the acquisition configuration menu. The first drop menu displayed permits selecting from any installed Sapera acquisition servers (installed acquisition hardware using Sapera drivers). The second drop menu permits selecting from the available input devices present on the selected server.

CCF File Selection

The acquisition configuration menu is also used to select the required camera configuration file for the connected camera. Sapera camera files contain timing parameters and video conditioning parameters. The default folder for camera configuration files is also used by the CamExpert utility to save user generated or modified camera files.

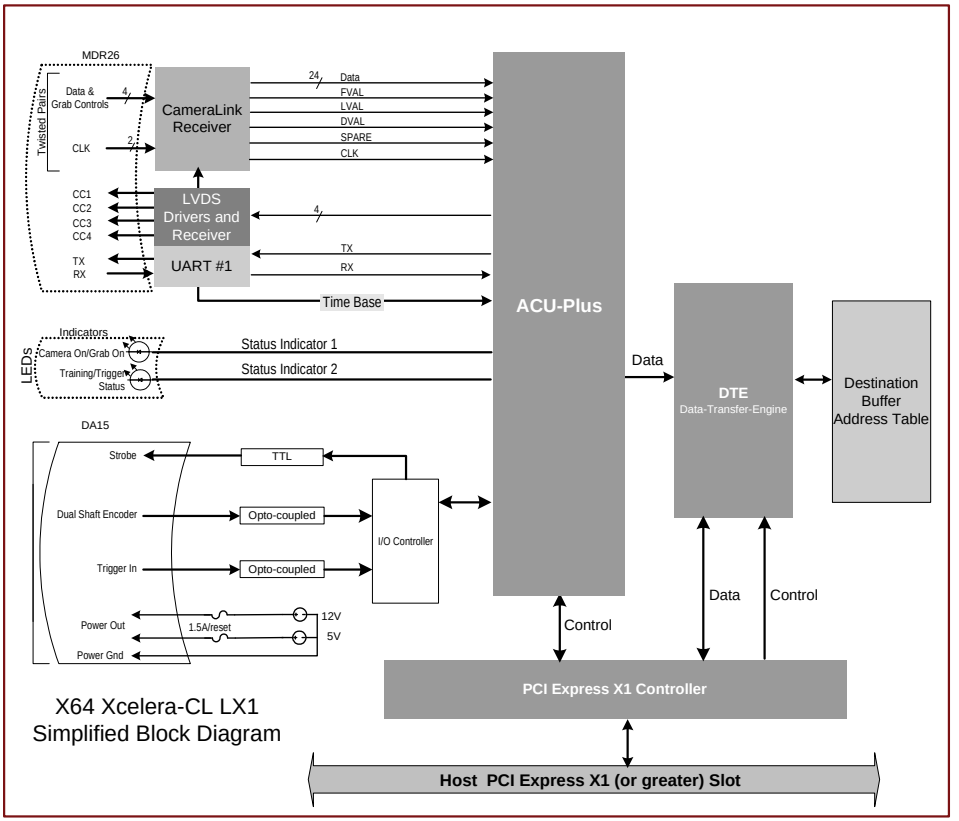
Use the Sapera CamExpert utility program to generate the camera configuration file based on timing and control parameters entered. The CamExpert live acquisition window allows immediate verification of those parameters. CamExpert reads both Sapera *.cca and *.cvi for backward compatibility with the original Sapera camera files.

Grab Demo Main Window

Refer to the Sapera LT User's Manual (OC-SAPM-USER), in section "Demos and Examples – Acquiring with Grab Demo", for more information on the Grab Demo.

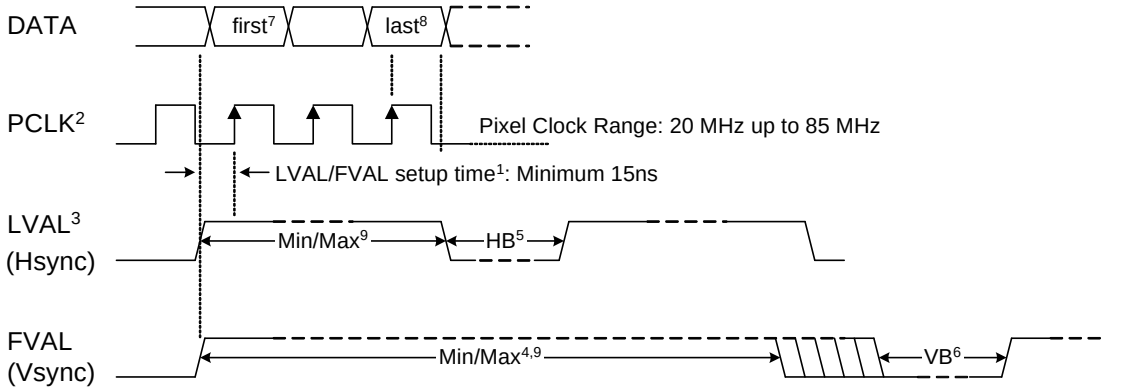
X64 Xcelera-CL LX1 Reference

Block Diagram



X64 Xcelera-CL LX1
Simplified Block Diagram

Acquisition Timing



- [1] The setup times for LVAL and FVAL are the same. Both must be high and stable before the rising edge of the Pixel Clock.
- [2] Pixel Clock must always be present.
- [3] LVAL must be active high to acquire camera data.
- [4] Minimum of 1.
- [5] HB - Horizontal Blanking:

  Minimum: 4 clocks/cycle
  Maximum: no limits

- [6] VB - Vertical Blanking:

  Minimum: 1 line
  Maximum: no limits

- [7] First Active Pixel (unless otherwise specified in the CCA file – "Horizontal Back invalid = x" where 'x' defines the number of pixels to be skipped).
- [8] Last Active Pixel – defined in the CCA file under "Horizontal active = y" – where 'y' is the total number of active pixels per tap.
- [9] Maximum Valid Data:
  - 8-bits/pixel, 16 Million Pixels/line (LVAL)
  - 16-bits/pixel, 8 Million Pixels/line (LVAL)
  - 32-bits/pixel, 4 Million pixels/line (LVAL)
  - 16 Million lines (FVAL)

Line Trigger Source Selection for Linescan Applications

Linescan imaging applications require some form of external event trigger to synchronize linescan camera exposures to the moving object. This synchronization signal is either an external trigger source (one exposure per trigger event) or a shaft encoder source composed of a single or dual phase (quadrature) signal. The X64 Xcelera-CL LX1 shaft encoder inputs provide additional functionality with pulse drop or pulse multiply support.

The following table describes the line trigger source types supported by the X64 Xcelera-CL LX1. Refer to the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00) for descriptions of the Sapera parameters.

CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE – Parameter Values Specific to the X64 Xcelera-CL LX1

PRM Value	Active Shaft Encoder Input
0	Default
1	Use phase A
2	Use phase B
3	Use phase A & B
4	From Board Sync
5	Phase A & B, shaft encoder after pulse drop/multiply output to Board Sync
6	Phase A & B, camera line trigger output to Board Sync
7	Phase A & B, camera line trigger output to Board Sync only while grabbing

CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE full description relative to trigger type and X64 Xcelera-CL LX1 configuration used:

PRM Value	Xcelera-CL LX1 configuration & camera input used	External Line Trigger Signal used	External Shaft Encoder Signal used
		if CORACQ_PRM_EXT_LINE_ TRIGGER_ENABLE = *true*	*if* CORACQ_PRM_SHAFT_ ENCODER_ENABLE =*true*
0	Camera #1	Shaft Encoder Phase A	Shaft Encoder Phase A
1	Camera #1	Shaft Encoder Phase A	Shaft Encoder Phase A
2	Camera #1	Shaft Encoder Phase B	Shaft Encoder Phase B
3, 5, 6, 7	Camera #1	n/a	Shaft Encoder Phase A & B
4	Camera #1	From Board Sync	From Board Sync

- See "J10: DB15 Female External Signals Connector" on page **69** for shaft encoder input connector details.
- See "J9: Board Sync" on page 74 for more details.

CVI/CCF File Parameters Used

- External Line Trigger Source = prm value
- External Line Trigger Enable = true/false
- Shaft Encoder Enable = true/false

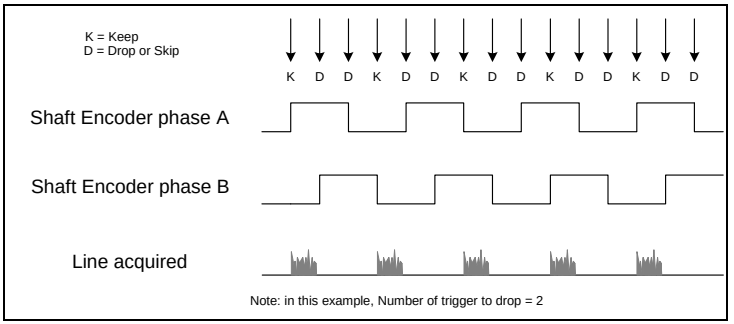
Shaft Encoder Interface Timing

Connector J10, Dual Balanced Shaft Encoder Inputs:

- See "J10: DB15 Female External Signals Connector" on page **69** for connector signal details.
- Input 1: Pin 2 (Phase A +) & Pin 10 (Phase A -)
- Input 2: Pin 3 (Phase B +) & Pin 11 (Phase B -)

Web inspection systems with variable web speeds typically provide one or two synchronization signals from a web mounted encoder to coordinate trigger signals. These trigger signals are used by the acquisition linescan camera. The X64 Xcelera-CL LX1 supports single or dual shaft encoder signals. Dual encoder signals are typically 90 degrees out of phase relative to each other and provide greater web motion resolution.

When enabled, the camera is triggered and acquires one scan line for each shaft encoder pulse edge. To optimize the web application, a second Sapera parameter defines the number of triggers to skip between valid acquisition triggers. The figure below depicts a system where a valid camera trigger is any pulse edge from either shaft encoder signal. After a trigger the two following triggers are ignored (as defined by the Sapera pulse drop parameter).



Note that camera file parameters are best modified by using the Sapera CamExpert program.

CVI/CCF File Parameters Used

Shaft Encoder Enable = X, where:

- If X = 1, Shaft Encoder is enabled
- If X = 0, Shaft Encoder is disabled

Shaft Encoder Pulse Drop = X, where:

- X = number of trigger pulses ignored between valid triggers

For information on camera configuration files see the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

Virtual Frame Trigger for Linescan Cameras

When using linescan cameras a frame buffer is allocated in host system memory to store captured video lines. To control when a video line is stored as the first line in this "virtual" frame buffer, an external frame trigger signal is used. The number of lines sequentially grabbed and stored in the virtual frame buffer is controlled by the Sapera vertical cropping parameter.

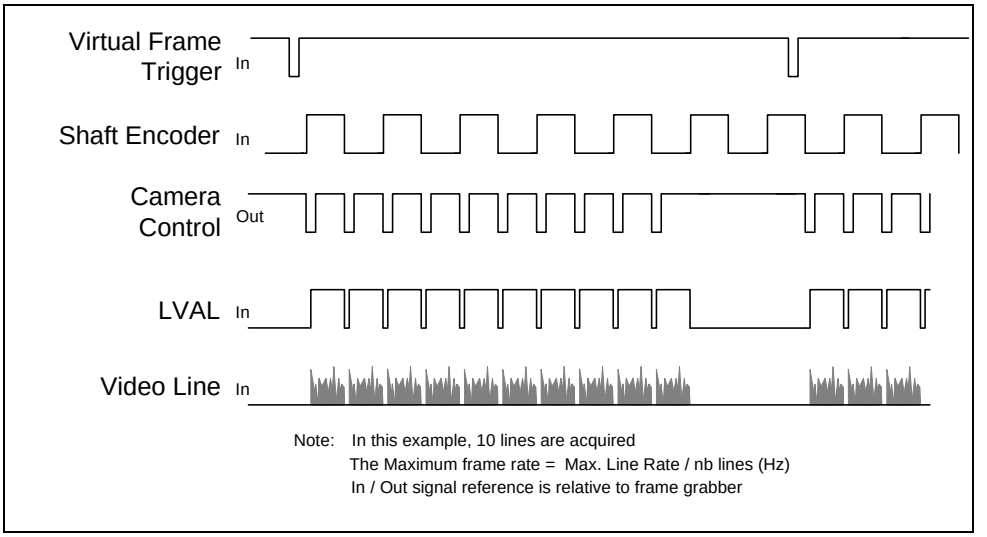
Virtual Frame Trigger Timing Diagram

The following timing diagram shows an example of grabbing 10 video lines from a linescan camera and the use of a virtual frame trigger to define when a video line is stored at the beginning of the virtual frame buffer. The virtual frame trigger signal (generated by some external event) is input on the X64 Xcelera-CL LX1 external trigger input.

- **Virtual frame trigger** can be 24V industry standard, TTL 5V or RS-422 and be rising or falling edge active, active high or low, or double pulse rising or falling edge.
- **Virtual frame trigger** control is configured for rising edge trigger in this example.
- **Virtual frame trigger** connects to the X64 Xcelera-CL LX1 via the External Trigger Input balanced inputs on connector J10, pin 1 (+) and 9 (-).
- After the X64 Xcelera-CL LX1 receives a virtual frame trigger, the camera control signal is output to the camera to trigger 'n' lines of video as per the defined virtual frame size.
- The camera control signal is either based on timing controls input on one or both X64 Xcelera-CL LX1 shaft encoder inputs (see "J10: DB15 Female External Signals Connector" on page **69** pinout) or an internal X64 Xcelera-CL LX1 clock.
- The number of lines captured is specified by the Sapera vertical cropping parameter.

Synchronization Signals for a Virtual Frame of 10 Lines.

The following timing diagram shows the relationship between an External Frame Trigger input, External Shaft Encoder input (one phase used with the second terminated), and camera control output to the camera.



CVI File (VIC) Parameters Used

The VIC parameters listed below provide the control functionality for virtual frame trigger. Applications either load pre-configured .cvi files or change VIC parameters directly during runtime.

Note that camera file parameters are best modified by using the Sapera CamExpert program.

External Frame Trigger Enable = X, where: (with Virtual Frame Trigger enabled)

- If X = 1, External Frame Trigger is enabled
- If X = 0, External Frame Trigger is disabled

External Frame Trigger Detection = Y, where: (with Virtual Frame Trigger edge select)

- If Y= 1, External Frame Trigger is active low
- If Y= 2, External Frame Trigger is active high
- If Y= 4, External Frame Trigger is active on rising edge
- If Y= 8, External Frame Trigger is active on falling edge
- If Y= 32, External Frame Trigger is dual-input rising edge
- If Y= 64, External Frame Trigger is dual-input falling edge

External Frame Trigger Level = Z, where: (with Virtual Frame Trigger signal type)

- If Z= 2, External Frame Trigger is a RS-422 signal

For information on camera files see the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

Acquisition Methods

Sapera acquisition methods define the control and timing of the camera and frame grabber board. Various methods are available, grouped as:

- Camera Trigger Methods (method 1 and 2 supported)
- Camera Reset Methods (method 1 supported)
- Line Integration Methods (method 1 through 4, 7 supported)
- Time Integration Methods (method 1 through 9 supported)
- Strobe Methods (method 1 through 4 supported)

Refer to the Sapera LT Acquisition Parameters Reference manual (OC-SAPM-APR00) for detailed information concerning camera and acquisition control methods.

Trigger To Image Reliability

Trigger-to-image reliability incorporates all stages of image acquisition inside an integrated controller to increase reliability and simplify error recovery. The trigger-to-image reliability model brings together all the requirements for image acquisition to a central management unit. These include signals to control camera timing, on-board FIFO memory to compensate for PCI bus latency, and comprehensive error notification. Whenever the X64 Xcelera-CL LX1 detects a problem, the user application is immediately informed and can take appropriate action to return to normal operation.

The X64 Xcelera-CL LX1 is designed with a robust ACU (Acquisition and Control Unit). The ACU monitors in real-time, the acquisition state the input plus the DTE (Data Transfer Engine), which transfers image data from on-board FIFO into PC memory. In general these management processes are transparent to end-user applications. With the X64 Xcelera-CL LX1, applications ensure trigger-to-image reliability by monitoring events and controlling transfer methods as described below:

Supported Events and Transfer Methods

The following acquisition and transfer events are supported. Event monitoring is a major component to the Trigger-to-Image Reliability framework.

Acquisition Events

Acquisition events are related to the acquisition module. They provide feedback on the image capture phase.

- **External Trigger** (Used/Ignored)
  Generated when the external trigger pin is asserted, usually indicating the start of the acquisition process. There are 2 types of external trigger events: 'Used' or 'Ignored'. Following an external trigger, if the event generates a captured image, an External Trigger Used event will be generated (CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER).
  If there is no captured image, an External Trigger Ignored event will be generated (CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_IGNORED). An external trigger event will be ignored if the rate at which the events are received are higher than the possible frame rate of the camera.
- **Start of Frame**
  Event generated, during acquisition, when the video frame start is detected by the board acquisition hardware. The Sapera event value is CORACQ_VAL_EVENT_TYPE_START_OF_FRAME.
- **End of Frame**
  Event generated, during acquisition, when the video frame end is detected by the board acquisition hardware. The Sapera event value is CORACQ_VAL_EVENT_TYPE_END_OF_FRAME.
- **Data Overflow**
  The Data Overflow event indicates that there is not enough bandwidth for the acquired data to be transferred without loss. This is usually caused by limitations of the acquisition module and should never occur.
  The Sapera event value is CORACQ_VAL_EVENT_TYPE_DATA_OVERFLOW.
- **Frame Valid**
  Event generated when the video frame start is detected by the board acquisition hardware. Acquisition does not need to be started, therefore this event can verify a valid signal is connected. The Sapera event value is CORACQ_VAL_EVENT_TYPE_VERTICAL_SYNC.
- **Pixel Clock** (Present/Absent)
  Event generated on the transition from detecting or not detecting a pixel clock signal. The Sapera event values are CORACQ_VAL_EVENT_TYPE_NO_PIXEL_CLK and CORACQ_VAL_EVENT_TYPE_PIXEL_CLK.
- **Frame Lost**
  The Frame Lost event indicates that an acquired image overflowed input FIFO memory before the FIFO content could be transferred to host memory. An example of this case would be if the image transfer from the on-board FIFO to host PC memory cannot be sustained due to bus

bandwidth issues.
The Sapera event value is CORACQ_VAL_EVENT_TYPE_FRAME_LOST.

- **Vertical Timeout**
  This event indicates a timeout situation where a camera fails to output a video frame after a trigger. The Sapera event value is CORACQ_VAL_EVENT_VERTICAL_TIMEOUT.

Transfer Events

Transfer events are the ones related to the transfer module. Transfer events provide feedback on image transfer from on-board FIFO to PC memory frame buffers.

- **Start of Frame**
  The Start of Frame event is generated when the first image pixel is transferred from on-board FIFO into PC memory.
  The Sapera event value is CORXFER_VAL_EVENT_TYPE_START_OF_FRAME.
- **End of Frame**
  The End of Frame event is generated when the last image pixel is transferred from on-board FIFO into PC memory.
  The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_FRAME.
- **End of Line**
  The End of Line event is generated after a video line is transferred to a PC buffer.
  The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_LINE.
- **End of N Lines**
  The End of N Lines event is generated after a set number of video lines are transferred to a PC buffer. The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_NLINES.
- **End of Transfer**
  The End of Transfer event is generated at the completion of the last image being transferred from on-board FIFO into PC memory. To complete a transfer, a stop must be issued to the transfer module (if transfers are already in progress). If a transfer of a fixed number of frames was requested, the transfer module will stop transfers automatically. The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_TRANSFER.

Trigger Signal Validity

External trigger signal noise is easily ignored by the ACU with its programmable debounce control. A parameter is programmed for the minimum pulse duration considered as a valid external trigger pulse. Refer to “Note 1: External Trigger Input Specifications” on page 70 for more information.

Supported Transfer Cycling Methods

The X64 Xcelera-CL LX1 supports the following transfer cycle modes which are either synchronous or asynchronous. These definitions are from the Sapera Basic Reference manual.

- CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_WITH_TRASH
  Before cycling to the next buffer in the list, the transfer device will check the next buffer's state. If its state is full, the transfer will be done in the trash buffer which is defined as the last buffer in the list; otherwise, it will occur in the next buffer. After a transfer to the trash buffer is done, the transfer device will check again the state of the next buffer. If it is empty, it will transfer to this buffer otherwise it will transfer again to the trash buffer.

- CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_NEXT_EMPTY_WITH_TRASH
  Before cycling to the next buffer in the list, the transfer device will check the next buffer's state. If its state is full, the next buffer will be skipped, and the transfer will be done in the trash buffer, which is defined as the last buffer in the list; otherwise it will occur in the next buffer. After a transfer to the trash is done, the transfer device will check the next buffer in the list, if its state is empty, it will transfer to this buffer otherwise it will skip it, and transfer again to the trash buffer.
- CORXFER_VAL_CYCLE_MODE_ASYNCHRONOUS
  The transfer device cycles through all buffers in the list without concern about the buffer state.

X64 Xcelera-CL LX1 Supported Parameters

The tables below describe the Sapera capabilities supported by the X64 Xcelera-CL LX1 (that is, default firmware is loaded). Unless specified, each capability applies to both boards or all mode configurations and all acquisition modes.

The information here is subject to change. Capabilities should be verified by the application because new board driver releases may change product specifications.

Specifically the X64 Xcelera-CL LX1 family is described in Sapera as:

- Board Server: Xcelera-CL_LX1_1
- Acquisition Module: *dependent on firmware used*

Camera Related Capabilities

Capability	Values
CORACQ_CAP_CONNECTOR_TYPE	CORACQ_VAL_CONNECTOR_TYPE_CAMLINK (0x2)
CORACQ_CAP_CONNECTOR_CAMLINK (Pin – 01)	CORACQ_VAL_SIGNAL_NAME_NO_CONNECT (0x1) CORACQ_VAL_SIGNAL_NAME_PULSE0 (0x8) CORACQ_VAL_SIGNAL_NAME_PULSE1 (0x10) CORACQ_VAL_SIGNAL_NAME_GND (0x4000)
CORACQ_CAP_CONNECTOR_CAMLINK (Pin – 02)	CORACQ_VAL_SIGNAL_NAME_NO_CONNECT (0x1) CORACQ_VAL_SIGNAL_NAME_PULSE0 (0x8) CORACQ_VAL_SIGNAL_NAME_PULSE1 (0x10) CORACQ_VAL_SIGNAL_NAME_GND (0x4000)
CORACQ_CAP_CONNECTOR_CAMLINK (Pin – 03)	CORACQ_VAL_SIGNAL_NAME_NO_CONNECT (0x1) CORACQ_VAL_SIGNAL_NAME_PULSE0 (0x8) CORACQ_VAL_SIGNAL_NAME_PULSE1 (0x10) CORACQ_VAL_SIGNAL_NAME_GND (0x4000)
CORACQ_CAP_CONNECTOR_CAMLINK (Pin – 04)	CORACQ_VAL_SIGNAL_NAME_NO_CONNECT (0x1)

Camera Related Parameters

Parameter		Values
CORACQ_PRM_CHANNEL	*Base Mono:* *Base Color RGB:*	1 1
CORACQ_PRM_FRAME		CORACQ_VAL_FRAME_PROGRESSIVE (0x2)
CORACQ_PRM_INTERFACE		CORACQ_VAL_INTERFACE_DIGITAL (0x2)
CORACQ_PRM_SCAN		CORACQ_VAL_SCAN_AREA (0x1) CORACQ_VAL_SCAN_LINE (0x2)
CORACQ_PRM_SIGNAL		CORACQ_VAL_SIGNAL_DIFFERENTIAL (0x2)
CORACQ_PRM_VIDEO	*All Mono:* *All Color RGB:*	CORACQ_VAL_VIDEO_MONO (0x1) CORACQ_VAL_VIDEO_RGB (0x8)
CORACQ_PRM_PIXEL_DEPTH		
	Base Mono:	8 bits, CORDATA_FORMAT_MONO8 10 bits, CORDATA_FORMAT_MONO10 12 bits, CORDATA_FORMAT_MONO12 14 bits, CORDATA_FORMAT_MONO14 16 bits, CORDATA_FORMAT_MONO16
	Base Color RGB:	8 bits, CORDATA_FORMAT_COLORNI8
CORACQ_PRM_VIDEO_STD		CORACQ_VAL_VIDEO_STD_NON_STD (0x1)
CORACQ_PRM_FIELD_ORDER		CORACQ_VAL_FIELD_ORDER_NEXT_FIELD (0x4)
CORACQ_PRM_HACTIVE		min = 1 pixel max = 16777215 pixel step = 1 pixel
CORACQ_PRM_HSYNC		min = 4 pixel max = 4294967295 pixel step = 1 pixel
CORACQ_PRM_VACTIVE		min = 1 line max = 16777215 line step = 1 line
CORACQ_PRM_VSYNC		min = 0 line max = 4294967295 line step = 1 line
CORACQ_PRM_HFRONT_INVALID		min = 0 pixel max = 16777215 pixel step = 1 pixel
CORACQ_PRM_HBACK_INVALID		min = 0 pixel max = 16777215 pixel step = 1 pixel
CORACQ_PRM_VFRONT_INVALID		min = 0 line max = 16777215 line step = 1 line
CORACQ_PRM_VBACK_INVALID		min = 0 line max = 16777215 line step = 1 line
CORACQ_PRM_PIXEL_CLK_SRC		CORACQ_VAL_PIXEL_CLK_SRC_EXT (0x2)
CORACQ_PRM_PIXEL_CLK_EXT		min = 20000000 Hz max = 85000000 Hz step = 1 Hz

CORACQ_PRM_SYNC		CORACQ_VAL_SYNC_SEP_SYNC (0x4)
CORACQ_PRM_HSYNC_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1)
CORACQ_PRM_VSYNC_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1)
CORACQ_PRM_FRAME_INTEGRATE_METHOD		Not available
CORACQ_PRM_FRAME_INTEGRATE_POLARITY		Not available
CORACQ_PRM_TIME_INTEGRATE_METHOD		CORACQ_VAL_TIME_INTEGRATE_METHOD_1 (0x1) CORACQ_VAL_TIME_INTEGRATE_METHOD_2 (0x2) CORACQ_VAL_TIME_INTEGRATE_METHOD_3 (0x4) CORACQ_VAL_TIME_INTEGRATE_METHOD_4 (0x8) CORACQ_VAL_TIME_INTEGRATE_METHOD_5 (0x10) CORACQ_VAL_TIME_INTEGRATE_METHOD_6 (0x20) CORACQ_VAL_TIME_INTEGRATE_METHOD_7 (0x40) CORACQ_VAL_TIME_INTEGRATE_METHOD_8 (0x80)
CORACQ_PRM_CAM_TRIGGER_METHOD		CORACQ_VAL_CAM_TRIGGER_METHOD_1 (0x1) CORACQ_VAL_CAM_TRIGGER_METHOD_2 (0x2)
CORACQ_PRM_CAM_TRIGGER_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_CAM_TRIGGER_DURATION		min = 1 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_CAM_RESET_METHOD		CORACQ_VAL_CAM_RESET_METHOD_1 (0x1)
CORACQ_PRM_CAM_RESET_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_CAM_RESET_DURATION		min = 1 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_CAM_NAME		Default Area Scan
CORACQ_PRM_LINE_INTEGRATE_METHOD		CORACQ_VAL_LINE_INTEGRATE_METHOD_1 (0x1) CORACQ_VAL_LINE_INTEGRATE_METHOD_2 (0x2) CORACQ_VAL_LINE_INTEGRATE_METHOD_3 (0x4) CORACQ_VAL_LINE_INTEGRATE_METHOD_4 (0x8) CORACQ_VAL_LINE_INTEGRATE_METHOD_7 (0x40)
CORACQ_PRM_LINE_TRIGGER_METHOD		CORACQ_VAL_LINE_TRIGGER_METHOD_1 (0x1)
CORACQ_PRM_LINE_TRIGGER_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_LINE_TRIGGER_DELAY		min = 0 µs max = 65535 µs step = 1 µs
CORACQ_PRM_LINE_TRIGGER_DURATION		min = 0 µs max = 65535 µs step = 1 µs
CORACQ_PRM_TAPS	*Bass Mono:* *Base Color RGB:*	max = 3 taps (for 3 taps, segmented only) max = 2 taps
CORACQ_PRM_TAP_OUTPUT		CORACQ_VAL_TAP_OUTPUT_ALTERNATE (0x1) CORACQ_VAL_TAP_OUTPUT_SEGMENTED (0x2) CORACQ_VAL_TAP_OUTPUT_PARALLEL (0x4)
CORACQ_PRM_TAP_1_DIRECTION	*All mono and color versions*	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)

CORACQ_PRM_TAP_2_DIRECTION	*All mono and color versions*	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_3_DIRECTION	*Only forBase Mono*	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_PIXEL_CLK_DETECTION		CORACQ_VAL_RISING_EDGE (0x4)
CORACQ_PRM_CHANNELS_ORDER		CORACQ_VAL_CHANNELS_ORDER_NORMAL (0x1)
CORACQ_PRM_LINESCAN_DIRECTION		Not available
CORACQ_PRM_LINESCAN_DIRECTION_POLARITY		Not available
CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MIN		1 Hz
CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MAX		16777215 Hz
CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MIN		1 µs
CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MAX		65535000 µs
CORACQ_PRM_TIME_INTEGRATE_PULSE1_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_TIME_INTEGRATE_PULSE1_DELAY		min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_PULSE1_DURATION		min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_PULSE0_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_TIME_INTEGRATE_PULSE0_DELAY		min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_PULSE0_DURATION		min = 1 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_LINE_INTEGRATE_PULSE1_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_LINE_INTEGRATE_PULSE1_DELAY		min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_LINE_INTEGRATE_PULSE1_DURATION		min = 1 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_LINE_INTEGRATE_PULSE0_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_LINE_INTEGRATE_PULSE0_DELAY		min = 0 µs max = 65535 µs step = 1 µs
CORACQ_PRM_LINE_INTEGRATE_PULSE0_DURATION		min = 1 µs max = 65535000 µs step = 1 µs

CORACQ_PRM_CONNECTOR_LINE_INTEGRATE_INPUT	Connector #1, type 2, pin #1
CORACQ_PRM_CAMLINK_CONFIGURATION	
Bass Mono and Base Color RGB	CORACQ_VAL_CAMLINK_CONFIGURATION_BASE (0x1)
CORACQ_PRM_DATA_VALID_ENABLE	TRUE / FALSE
CORACQ_PRM_DATA_VALID_POLARITY	CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_TIMESLOT	CORACQ_VAL_TIMESLOT_1 (0x1)
CORACQ_PRM_BAYER_ALIGNMENT	Not available
CORACQ_PRM_CAM_CONTROL_DURING_READOUT	TRUE / FALSE

VIC Related Parameters

Parameter		Values
CORACQ_PRM_CAMSEL	*all mono modes:*	CAMSEL_MONO = from 0 to 0
	all color modes:	CAMSEL_RGB = from 0 to 0
CORACQ_PRM_PIXEL_MASK		Not available
CORACQ_PRM_CROP_LEFT		min = 0 pixel max = 16777215 pixel step = 8 pixel
CORACQ_PRM_CROP_TOP		min = 0 line max = 16777215 line step = 1 line
CORACQ_PRM_CROP_WIDTH		min = 8 pixel max = 16777215 pixel step = 8 pixel
CORACQ_PRM_CROP_HEIGHT		min = 1 line max = 16777215 line step = 1 line
CORACQ_PRM_SCALE_HORZ		Not available
CORACQ_PRM_SCALE_VERT		Not available
CORACQ_PRM_DECIMATE_METHOD		CORACQ_VAL_DECIMATE_DISABLE (0x1)
CORACQ_PRM_LUT_ENABLE		Not available
CORACQ_PRM_STROBE_ENABLE		TRUE FALSE
CORACQ_PRM_STROBE_METHOD		CORACQ_VAL_STROBE_METHOD_1 (0x1) CORACQ_VAL_STROBE_METHOD_2 (0x2) CORACQ_VAL_STROBE_METHOD_3 (0x4) CORACQ_VAL_STROBE_METHOD_4 (0x8)
CORACQ_PRM_STROBE_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_STROBE_DURATION		min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_STROBE_DELAY		min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_FRAME_INTEGRATE_ENABLE		Not available

CORACQ_PRM_FRAME_INTEGRATE_COUNT	Not available
CORACQ_PRM_TIME_INTEGRATE_ENABLE	TRUE FALSE
CORACQ_PRM_TIME_INTEGRATE_DURATION	min = 1 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_CAM_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_CAM_RESET_ENABLE	TRUE FALSE
CORACQ_PRM_OUTPUT_FORMAT	
all mono modes:	CORACQ_VAL_OUTPUT_FORMAT_MONO8 CORACQ_VAL_OUTPUT_FORMAT_MONO16
base color RGB mode	CORACQ_VAL_OUTPUT_FORMAT_RGB8888
CORACQ_PRM_EXT_TRIGGER_ENABLE	CORACQ_VAL_EXT_TRIGGER_OFF (0x1) CORACQ_VAL_EXT_TRIGGER_ON (0x8)
CORACQ_PRM_VIC_NAME	Default Area Scan
CORACQ_PRM_EXT_TRIGGER_DETECTION	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2) CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8)
CORACQ_PRM_VSYNC_TIMEOUT	Not available
CORACQ_PRM_VSYNC_REF	CORACQ_VAL_SYNC_REF_END (0x2)
CORACQ_PRM_HSYNC_REF	CORACQ_VAL_SYNC_REF_END (0x2)
CORACQ_PRM_LINE_INTEGRATE_ENABLE	TRUE FALSE
CORACQ_PRM_LINE_INTEGRATE_DURATION	min = 1 pixel max = 16777215 pixel step = 1 pixel
CORACQ_PRM_LINE_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_FRAME_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_FRAME_TRIGGER_DETECTION	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2) CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8) CORACQ_VAL_DOUBLE_PULSE_RISING_EDGE (0x20) CORACQ_VAL_DOUBLE_PULSE_FALLING_EDGE (0x40)
CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_LINE_TRIGGER_DETECTION	CORACQ_VAL_RISING_EDGE (0x4)
CORACQ_PRM_SNAP_COUNT	Default = 1 frame
CORACQ_PRM_INT_LINE_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_INT_LINE_TRIGGER_FREQ	Default = 5000 Hz
CORACQ_PRM_BIT_ORDERING	CORACQ_VAL_BIT_ORDERING_STD (0x1)
CORACQ_PRM_EXT_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_STROBE_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1)

CORACQ_PRM_EXT_FRAME_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_EXT_LINE_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_INT_LINE_TRIGGER_FREQ_MIN	245 Hz
CORACQ_PRM_INT_LINE_TRIGGER_FREQ_MAX	500000 Hz
CORACQ_PRM_MASTER_MODE	Not available
CORACQ_PRM_SHAFT_ENCODER_DROP	min = 0 tick max = 255 tick step = 1 tick
CORACQ_PRM_SHAFT_ENCODER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_TRIGGER_FRAME_COUNT	Default = 1 frame
CORACQ_PRM_INT_FRAME_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_INT_FRAME_TRIGGER_FREQ	min = 1 milli-Hz max = 1073741823 milli-Hz step = 1 milli-Hz
CORACQ_PRM_STROBE_DELAY_2	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_FRAME_LENGTH	CORACQ_VAL_FRAME_LENGTH_FIX (0x1) CORACQ_VAL_FRAME_LENGTH_VARIABLE (0x2)
CORACQ_PRM_FLIP	CORACQ_VAL_FLIP_HORZ (0x1)
CORACQ_PRM_EXT_TRIGGER_DURATION	min = 0 µs max = 255 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_DELAY	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_CAM_RESET_DELAY	min = 0 µs max = 0 µs step = 1 µs
CORACQ_PRM_CAM_TRIGGER_DELAY	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_SHAFT_ENCODER_LEVEL	CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_EXT_FRAME_TRIGGER_SOURCE	min = 0 max = 5 step = 1 See CORACQ_PRM_EXT_TRIGGER_SOURCE_STR
CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE (*)	min = 0 max = 7 step = 1 See CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE_STR
CORACQ_PRM_EXT_TRIGGER_SOURCE	min = 0 max = 5 step = 1 See CORACQ_PRM_EXT_TRIGGER_SOURCE_STR
CORACQ_PRM_SHAFT_ENCODER_MULTIPLY	min = 1 max = 32 step = (2**N)
CORACQ_PRM_PLANAR_INPUT_SOURCES	Not available

CORACQ_PRM_EXT_TRIGGER_DELAY	min = 0 max = 65535000 step = 1
CORACQ_PRM_EXT_TRIGGER_DELAY_TIME_BASE	CORACQ_VAL_TIME_BASE_LINE (0x4)
CORACQ_PRM_BAYER_DECODER_ENABLE	Not available
CORACQ_PRM_CAM_CONTROL_PULSE0_HD_ALIGN	Not available
CORACQ_PRM_CAM_CONTROL_PULSE1_HD_ALIGN	Not available
CORACQ_PRM_EXT_TRIGGER_IGNORE_DELAY	min = 0 max = 65535000 step = 1
CORACQ_PRM_CONTROL_SIGNAL_OUTPUT1	Not available
CORACQ_PRM_CONTROL_SIGNAL_OUTPUT2	Not available
CORACQ_PRM_EXT_TRIGGER_SOURCE_STR	[0] = Automatic [1] = From External Trigger [2] = Reserved [3] = From Board Sync [4] = To Board Sync [5] = Pulse to Board Sync
CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE_STR	[0] = Automatic [1] = From Shaft Encoder Phase A [2] = From Shaft Encoder Phase B [3] = From Shaft Encoder Phase A & B [4] = From Board Sync [5] = To Board Sync [6] = Pulse to Board Sync [7] = To Board Sync When Grabbing
CORACQ_PRM_VERTICAL_TIMEOUT_DELAY	min = 0 max = 16383000 step = 1
CORACQ_PRM_POCL_ENABLE	TRUE FALSE
CORACQ_PRM_CROP_ACTIVATION	Not available

ACQ Related Parameters

Parameter	Values
CORACQ_PRM_LABEL	
Base mono	CameraLink Base Mono #1
Base Color RGB	CameraLink Base Color RGB #1
CORACQ_PRM_EVENT_TYPE	CORACQ_VAL_EVENT_TYPE_START_OF_FRAME CORACQ_VAL_EVENT_TYPE_END_OF_FRAME CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER CORACQ_VAL_EVENT_TYPE_VERTICAL_SYNC CORACQ_VAL_EVENT_TYPE_NO_PIXEL_CLK CORACQ_VAL_EVENT_TYPE_PIXEL_CLK CORACQ_VAL_EVENT_TYPE_FRAME_LOST CORACQ_VAL_EVENT_TYPE_DATA_OVERFLOW CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_IGNORED CORACQ_VAL_EVENT_TYPE_VERTICAL_TIMEOUT
CORACQ_PRM_SIGNAL_STATUS	CORACQ_VAL_SIGNAL_HSYNC_PRESENT CORACQ_VAL_SIGNAL_VSYNC_PRESENT CORACQ_VAL_SIGNAL_PIXEL_CLK_PRESENT
CORACQ_PRM_DETECT_PIXEL_CLK	Not available
CORACQ_PRM_DETECT_HACTIVE	Available
CORACQ_PRM_DETECT_VACTIVE	Available
CORACQ_PRM_FLAT_FIELD_ENABLE	Not available
CORACQ_CAP_SERIAL_PORT_INDEX	Supported

Sapera Servers & Resources

Servers and Resources

The following table describes the X64 Xcelera-CL LX1

Servers	Resources			
Name	**Type**	**Name**	**Index**	**Description**
Xcelera-CL_LX1_1 (default Base firmware)	Acquisition	CameraLink Base Mono 1	0	Base configuration, monochrome Camera #1
		CameraLink Base RGB 1	1	Base configuration, color RGB Camera #1

Technical Specifications

X64 Xcelera-CL LX1 Board Specifications

X64 Xcelera-CL LX1 Dimensions

Approximately 3 in. (7.5 cm) wide by 4 in. (10 cm) high.

Digital Video Input & Controls

Input Type	Camera Link Specifications Rev 1.10 compliant; 1 Base
Common Pixel Formats	Camera Link tap configuration for 8, 10, 12, 14 and 16-bit mono, 24-bit RGB.
Tap Format Details	1 Tap – 8/10/12/14/16-bit mono 2 Taps – 8/10/12-bit mono 3 taps – 8-bit mono/RGB
Scanning	Area scan and Linescan: Progressive, Multi-Tap, Tap reversal, Segmented Tap Configuration, Alternate Tap Configuration
Scanning Directions	Left to Right, Right to Left, Up-Down, Down-Up From Top, From Middle, From Bottom
Resolution *note: these are X64 Xcelera-CL LX1 maximums, not Camera Link specifications*	Horizontal Minimum: 8 Pixels per tap (8-bits/pixel) Horizontal Maximum: 8-bits/pixel, 16 Million Pixels/line 16-bits/pixel, 8 Million Pixels/line 32-bits/pixel, 4 Million Pixels/line Vertical Minimum: 1 line Vertical Maximum: up to 16,000,000 lines—for area scan cameras infinite line count—for linescan cameras
Pixel Clock Range	20 MHz to 85 MHz as follows: 8-bit: 3 taps @ 85 MHz, any tap configuration 10/12-bit: 2 taps @ 85 MHz, any tap configuration 14/16-bit:1 tap @ 85 MHz, any tap configuration
Synchronization Minimums	Horizontal Sync minimum: 4 pixels Vertical Sync minimum: 1 line
Bandwidth to Host System	Approximately 185MB/s.
Serial Port	Supports communication speeds from 9600 to 115200 bps

Controls	Compliant with Teledyne DALSA Trigger-to-Image Reliability framework
	Comprehensive event notifications, (see "Trigger To Image Reliability" on page 46)
	Timing control logic for EXSYNC, PRIN and strobe signals
	Opto-coupled external trigger input programmable as active high or low (edge or level trigger, where pulse width minimum is 100ns)
	External trigger latency less than 1 µsec.
	TTL Strobe output
	Quadrature (AB) shaft-encoder inputs for external web synchronization (opto-coupler maximum frequency for any shaft encoder input is 200 KHz)

Host System Requirements

General System Requirements for the X64 Xcelera-CL LX1

- PCI Express x1; (x4 slot or x8 slot compatible — x16 slots require individual testing)
- On some computers the X64 Xcelera-CL LX1 installed in an x16 slot may function. The computer documentation or direct testing is required.

Operating System Support

- Windows XP, Windows Vista, Windows 7 (all versions in 32-bit or 64-bit)

Environment

Ambient Temperature:	10° to 50° C (operation) 0° to 70° C (storage)
Relative Humidity:	5% to 90% non-condensing (operating) 0% to 95% (storage)

Power Requirements

+3.3V:	0.48A (standby) 0.55A (during acquisition)
+12V:	0.02A (standby) 0.02A (during acquisition)

EMI Certifications

TELEDYNE DALSA
Everywhereyoulook™

EC & FCC DECLARATION OF CONFORMITY

We : Teledyne DALSA inc.
7075 Place Robert-Joncas, Suite 142,
St. Laurent, Quebec, Canada, H4M 2Z2

Declare under sole legal responsibility that the following products conform to the protection requirements of council directive 2004/108/EC on the approximation of the laws of member states relating to electromagnetic compatibility:

Xcelera-CL LX1

The products to which this declaration relates are in conformity with the following relevant harmonized standards, the reference numbers of which have been published in the Official Journal of the European Communities:

EN55022:2006, A1:2007
EN55024:1998, A1:2001, A2:2003
ENV50204:1995

Further declare under our sole legal responsibility that the product listed conforms to the code of federal regulations CFR 47 part 15 (2008), subpart B, for a class A product.

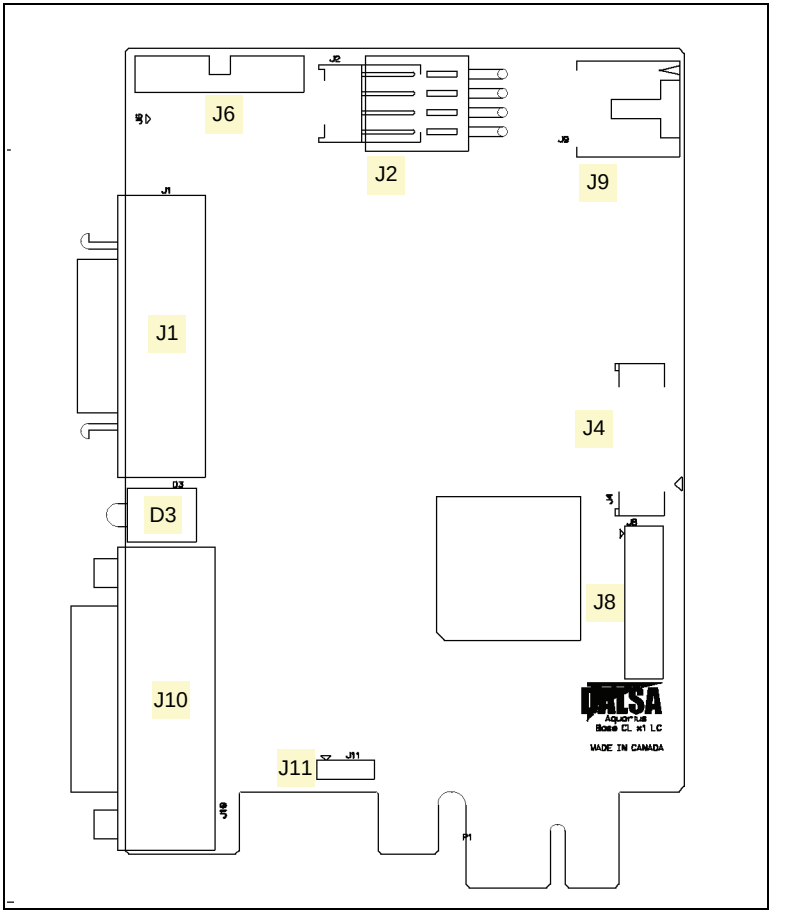
St. Laurent, Canada — Location
2012-04-09 — Date

Eric Carey

Eric Carey, ing.
Director,
Research and Development

Connector and Switch Locations

X64 Xcelera-CL LX1 Board Layout Drawing



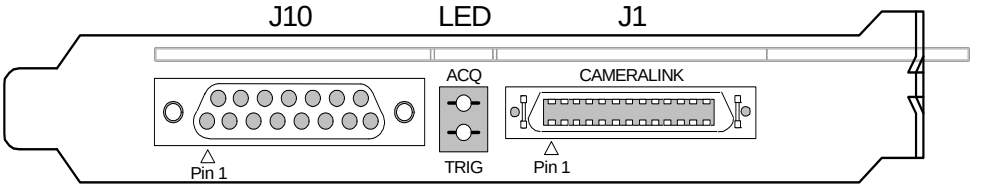
Connector, Switch, Jumper Description List

The following table lists components on the X64 Xcelera-CL LX1 board. Detailed information follows for connectors, switches and jumpers the end user may have need of.

Location	Description	Location	Description
J1	Camera Link Connector	J2	DC power to camera interface. Connect computer power cable to supply PoCL on J1.
J10	External Signals Connector	J11	Ext Trigger Switch point select
J9	Multi Board Sync	J4, J6	Reserved
J8 – pins 15/16	Normal Boot mode: shorting jumper ON (*default*) Safe Boot mode: shorting jumper OFF		

Connector and Switch Specifications

X64 Xcelera-CL LX1 End Bracket Detail



Connector Bracket

The hardware installation process is completed with the connection of a supported camera to the X64 Xcelera-CL LX1 board using Camera Link cables (see "Camera Link Cables" on page 79).

- The X64 Xcelera-CL LX1 board supports a camera with one Camera Link MDR-26 connector (one Base – see "Data Port Summary" on page 78 for information on Camera Link configurations).
- Connect the camera to the J1 connector with a Camera Link cable.

Note: If the camera is powered by the X64 Xcelera-CL LX1 (i.e. Power over Camera Link 'PoCL'), connect computer DC power to J2 and refer to PoCL notes for "J1: MDR 26-Pin Female Camera Link Connector" on page 67.

Contact Teledyne DALSA or browse our web site for the latest information on X64 Xcelera-CL LX1 supported cameras.

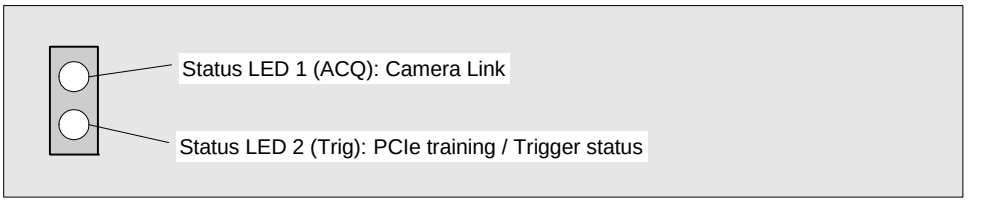
Configuration Jumper

J11: External Trigger Input Signal Switch Point

Selects the threshold voltage detected as a logic high signal. See "Note 1: External Trigger Input Specifications" on page 70.

1-2 Position (default)	2-3 Position
Logic Transition at ~2 volts (preferred for differential signals)	Logic Transition at ~10 volts

Status LEDs Functional Description



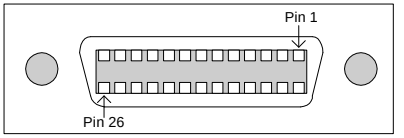
Status LED 1 (ACQ) Modes

- **Red**: No camera connected or camera has no power.
- **Green**: Camera connected and is ON. Camera clock detected. No line valid detected.
- **Slow Flashing Green** (~2 Hz): Camera Line Valid signal detected.
- **Fast Flashing Green** (~16 Hz): Acquisition in progress.

Status LED 2 (Trig) Modes

- ***Flashing red***: (At boot time)
  This indicates that the board PCIe interface was not trained properly (terminology defined by the PCI Express specification) by the computer. The board will not be detected in the computer in this condition. If this occurs, please contact Teledyne DALSA technical support.
- ***Green On/Flashing***: (While grabbing)
  The TRIG LED represents the status of the external trigger pin. This is based on the signal going through the DA-15 connector.
- ***Green On***: (While in Safe Boot Mode)
  Will stay steady On in green during safe boot mode operation.

J1: MDR 26-Pin Female Camera Link Connector



Name	Pin #	Type	Description
BASE_X0-	25	Input	Neg. Base Data 0
BASE_X0+	12	Input	Pos. Base Data 0
BASE_X1-	24	Input	Neg. Base Data 1
BASE_X1+	11	Input	Pos. Base Data 1
BASE_X2-	23	Input	Neg. Base Data 2
BASE_X2+	10	Input	Pos. Base Data 2
BASE_X3-	21	Input	Neg. Base Data 3
BASE_X3+	8	Input	Pos. Base Data 3
BASE_XCLK-	22	Input	Neg. Base Clock
BASE_XCLK+	9	Input	Pos. Base Clock
SERTC+	20	Output	Pos. Serial Data to Camera
SERTC-	7	Output	Neg. Serial Data to Camera
SERTFG-	19	Input	Neg. Serial Data to Frame Grabber
SERTFG+	6	Input	Pos. Serial Data to Frame Grabber
CC1-	18	Output	Neg. Camera Control 1
CC1+	5	Output	Pos. Camera Control 1
CC2+	17	Output	Pos. Camera Control 2
CC2-	4	Output	Neg. Camera Control 2
CC3-	16	Output	Neg. Camera Control 3
CC3+	3	Output	Pos. Camera Control 3
CC4+	15	Output	Pos. Camera Control 4
CC4-	2	Output	Neg. Camera Control 4
PoCL	1,26		+12 V (see note following this table)
GND	13, 14		Ground

Notes on Power over Camera Link (PoCL) support:

- Refer to Sapera ++ reference parameter SapAcquisition::SignalPoCLActive to enable PoCL.
- The PoCL state is maintained after a board reset.

Camera Link Camera Control Signal Overview

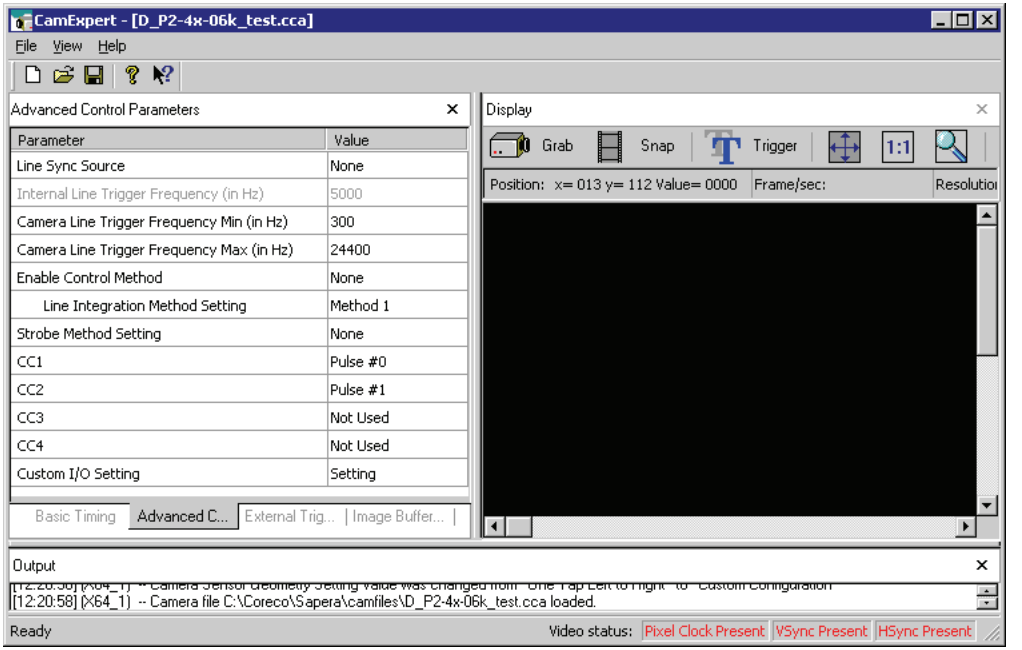
Four LVDS pairs are for general-purpose camera control, defined as camera inputs / frame grabber outputs by the Camera Link specification. These controls are on J1.

- Camera Control 1 (CC1)
- Camera Control 2 (CC2)
- Camera Control 3 (CC3)
- Camera Control 4 (CC4)

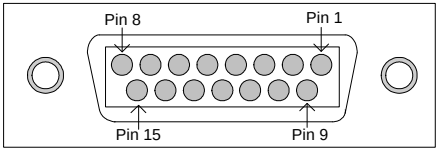
Each camera manufacture is free to define the signals input on any one or all four control signals. These control signals are used either as camera control pulses or as a static logic state. Control signals not required by the camera are simply assigned as not used. Refer to your camera's user manual for information on what control signals are required.

Note: The X64 Xcelera-CL LX1 pulse controller has a minimum resolution of 100ns for line trigger signals, and resolution of 1µs for all other signal.

The X64 Xcelera-CL LX1 can assign any camera control signal to the appropriate Camera Link control. The following screen shot shows the Sapera CamExpert dialog where Camera Link controls are assigned.



J10: DB15 Female External Signals Connector



Pin #	Pin Name	Type	Description
1	External Trigger+	Input	Opto-coupler Anode. (See note 1).
9	External Trigger-	Input	Opto-coupler Cathode. (See note 1)
2	Shaft Encoder Phase A+	Input	Phase A opto-coupler – Anode. (See note 2).
10	Shaft Encoder Phase A-	Input	Phase A opto-coupler – Cathode. (See note 2).
3	Shaft Encoder Phase B+	Input	Phase B opto-coupler – Anode.
11	Shaft Encoder Phase B-	Input	Phase B opto-coupler – Cathode.
4, 5, 8, 14	GND		Ground
12	Strobe	Output	Strobe signal output. (See note 3).
6, 13	12V	Output	DC power supplied by connecting the computer power supply to J2 (floppy disk power connector). See note 4
7, 15	5V	Output	DC power supplied by connecting the computer power supply to J2 (floppy disk power connector). See note 4

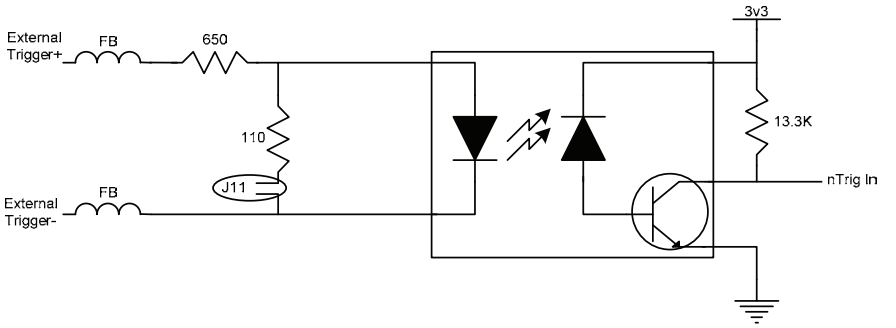
Optional Camera Power Cable OR-X1CC-XPOW1

This cable (available from Teledyne DALSA) connects +12Volts & GND from J10 to a 12 pin Hirose connector as shown in the following table.

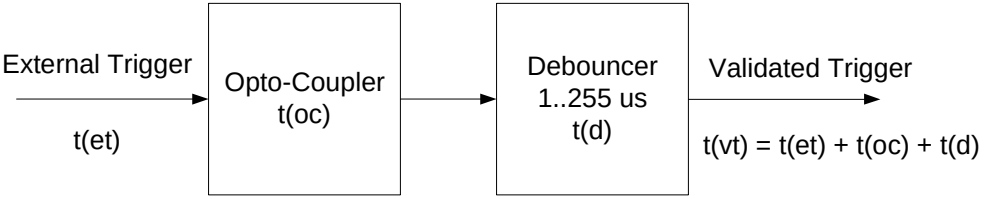
J10 pin number	Wire Identification	Hirose 12 pin number
14	Ground	1
13	+12 Volt	2

Note 1: External Trigger Input Specifications

The Trigger Input is opto-coupled and compatible to differential signals (RS-422) or single ended source signals. The following figure is typical for the External Trigger Input.



- For single ended signals, the External Trigger– pin is connected to ground. The switch point is ~2V by default to support TTL 5V signals and can be changed to switch at ~10V with SW2 to support 24V industry standard signals.
- For RS422 differential signals, switch point must be selected at ~2V.
- Maximum external signal input voltage is 26V, irrelevant of the selected switch point.
- The incoming trigger pulse is "debounced" to ensure that no voltage glitch is detected as a valid trigger pulse. This debounce circuit time constant can be programmed from 1µs to 255µs . Any pulse smaller than the programmed value is blocked and therefore not seen by the acquisition circuitry. If no debouncing value is specified (value of 0µs), the minimum value of 1µs will be used.
- Each input has a ferrite bead plus a 650 ohm series resistor on the opto-coupler anode.
- Maximum input signal frequency is 100 KHz.
- Opto-coupler response time is 0.5µs for a rising signal.
- Opto-coupler response time is 4.2µs for a falling signal.
- Refer to Sapera parameters:
  CORACQ_PRM_EXT_TRIGGER_SOURCE
  CORACQ_PRM_EXT_TRIGGER_ENABLE
  CORACQ_PRM_EXT_TRIGGER_LEVEL
  CORACQ_PRM_EXT_FRAME_TRIGGER_LEVEL
  CORACQ_PRM_EXT_TRIGGER_DETECTION
  CORACQ_PRM_EXT_TRIGGER_DURATION
- See also *.cvi file entries:
  External Trigger Level, External Frame Trigger Level, External Trigger Enable, External Trigger Detection.



External Trigger Input Validation & Delay

Let	t(et) = time of external trigger in µs t(vt) = time of validated trigger in µs t(oc) = time opto-coupler takes to change state t(d) = debouncing duration from 1 to 255µs
trigger high	For an active high external trigger, t(oc) = 0.5µs: t(vt) = t(et) + 0.5µs + t(d)
trigger low	For an active low external trigger, t(oc) = 4.2µs: t(vt) = t(et) + 4.2µs + t(d)

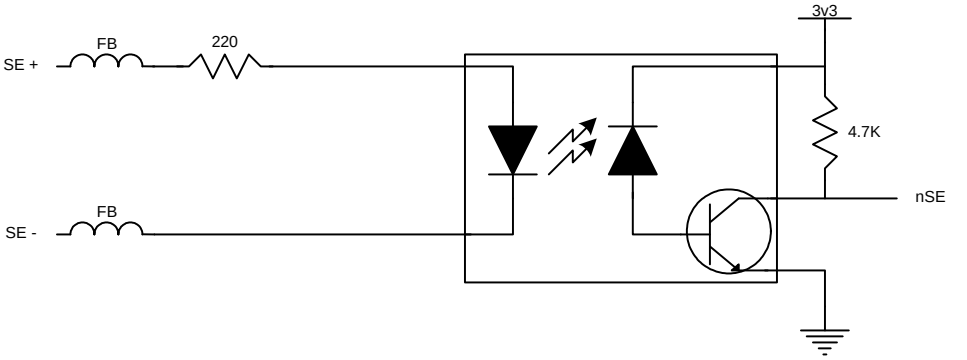
Note: Teledyne DALSA recommends using an active high external trigger to minimize the time it takes for the opto-coupler to change state. Specifically, the opto-coupler response time is 0.5µs for active high compared to 4.2µs for active low.

If the duration of the external trigger is > t(oc) + t(d), then a valid acquisition trigger is detected. Therefore, the external pulse with active high polarity must be at least 1.5µs (if debounce time is set to 1) in order to be acknowledged. Any pulse larger than 5.2µs is always considered valid.

It is possible to emulate an external trigger using the software trigger which is generated by a function call from an application.

Note 2: Shaft Encoder Input Specifications

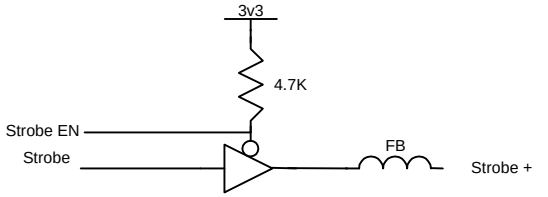
Dual Quadrature Shaft Encoder Inputs (phase A and phase B) are opto-coupled and able to connect to differential signals (RS-422) or single ended TTL 5V source signals. The following figure is typical for each input.



- For single ended TTL 5V signals, the SE– pin is connected to ground. The switch point is ~2V.
- Maximum external signal input voltage is 6V.
- Each input has a ferrite bead plus a 220 ohm series resistor on the opto-coupler anode.
- Maximum input signal frequency is 200 KHz.
- Opto-coupler response time is 0.25µs for a rising signal.
- Opto-coupler response time is 2.8µs for a falling signal.
- See "Line Trigger Source Selection for Linescan Applications" on page 41 for more information.
- Refer to Sapera parameters:
  CORACQ_PRM_SHAFT_ENCODER_ENABLE CORACQ_PRM_SHAFT_ENCODER_DROP
  or refer to CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE
  CORACQ_PRM_EXT_LINE_TRIGGER_DETECTION
  CORACQ_PRM_EXT_LINE_TRIGGER_LEVEL (fixed at RS-422)
  CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE
- See also *.cvi file entries:
  Shaft Encoder Enable, Shaft Encoder Pulse Drop
  or see External Line Trigger Enable, External Line Trigger Detection, External Line Trigger Level, External Line Trigger Source.

Note 3: Strobe Output Specifications

TTL Strobe output is provided. The following figure is typical for the strobe out.



- Strobe output uses a tri-state driver, enabled by software.
- Strobe output is 5V TTL level.
- Output has a ferrite bead.
- Maximum source current is 32mA typical.
- Maximum sink current is 32mA typical.
- Output switching is < 4.2ns typical.
- Refer to Sapera Strobe Methods parameters:
  CORACQ_PRM_STROBE_ENABLE
  CORACQ_PRM_STROBE_POLARITY
  CORACQ_PRM_STROBE_LEVEL
  CORACQ_PRM_STROBE_METHOD
  CORACQ_PRM_STROBE_DELAY
  CORACQ_PRM_STROBE_DURATION
- See also *.cvi file entries:
  Strobe Enable, Strobe Polarity, Strobe Level, Strobe Method, Strobe Delay, Strobe Duration.

Note 4: DC Power Details

- Connect the PC floppy drive power connector to J2 so as to supply DC power to a camera. Both 5Vdc and 12Vdc are available on J10.
- Both the 5Volt and 12Volt power pins have a 1.5A re-settable fuse on the board. If the fuse is tripped, turn off the host computer power. When the computer is turned on again, the fuse is automatically reset.

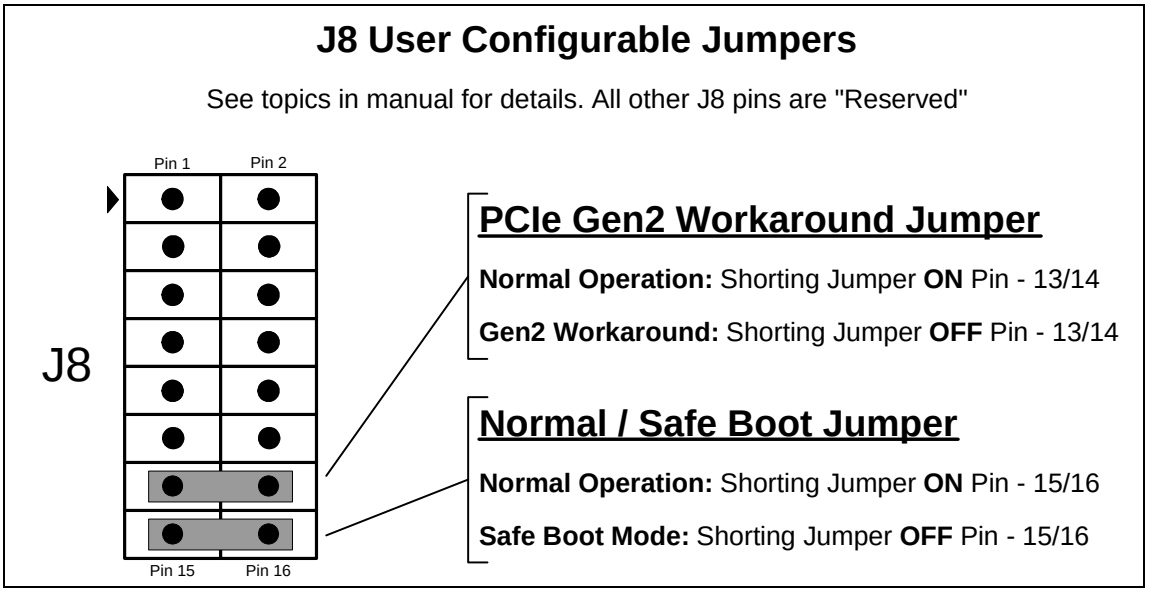
J9: Board Sync

Interconnects multiple X64 Xcelera boards to synchronize acquisitions to one trigger or event. The trigger source can be either an external signal or internal software trigger. The board receiving the trigger is the Master board, while the boards receiving the control signal from the Master board are Slaves.

- **Hardware Connection:** Interconnect two, three, or four X64 Xcelera boards via their J9 connector. The 4 pin cable is wired one to one — that is, no crossed wires. The cable must be as short as possible and the boards must be in the same system.
- **Master Board Software Setup:** Choose one X64 Xcelera as master. The Sapera parameter CORACQ_PRM_EXT_TRIGGER_SOURCE is used to setup the signal to send. *See section* "Line Trigger Source Selection for Linescan Applications" on page 41 and also the Sapera documentation for more details.
- **Slave Board Software Setup:** The Sapera parameter CORACQ_PRM_EXT_TRIGGER_SOURCE is set to *From Board Sync: see section* "Line Trigger Source Selection for Linescan Applications" on page 41.
- **Test Setup:** The control application starts the acquisition on all slave boards. The acquisition process is now waiting for the control signal from the master board. The master board acquisition is triggered and the acquisition start signal is sent to each slave board (with ~0.8µs delay max).

Contact Technical Support for additional information.

J8: Normal or Safe Boot Select Jumper



J8: GEN2 Slot (PCIe generation 2) Workaround Jumper

- Normal Mode: Shorting Jumper **ON** Pin **13/14** (see diagram above).
  Normal operation of the Xcelera-CL LX1.
- GEN2 Slot Workaround: Shorting Jumper **OFF** Pin – **13/14**.
  In computers with GEN2 slots and the Intel 5400 chipset. there have been circumstances where the board is not detected properly. This issue is identified by the status LED 2 that keeps on flashing red at boot time. In one example, with a Dell T5400 or T7400 computer, the following message was displayed by the computer BIOS:"Alert! Error initializing PCI Express slot".
- Therefore when using such a computer, with the jumper removed from the Xcelera, the computer should boot normally and the Xcelera should function. If this is not the case, please contact "Technical Support" on page 82 with details about your computer.

Camera Link Interface

Camera Link Overview

Camera Link is a communication interface for vision applications developed as an extension of National Semiconductor's Channel Link technology. The advantages of the Camera Link interface are that it provides a standard digital camera connection specification, a standard data communication protocol, and simpler cabling between camera and frame grabber.

The Camera Link interface simplifies the usage of increasingly diverse cameras and high signal speeds without complex custom cabling. For additional information concerning Camera Link, see **http://en.wikipedia.org/wiki/Camera_Link**.

Rights and Trademarks

Note: The following text is extracted from the Camera Link Specification 1.1 (January 2004).

The Automated Imaging Association (AIA), as sponsor of the Camera Link committee, owns the U.S. trademark registration for the Camera Link logo as a certification mark for the mutual benefit of the industry. The AIA will issue a license to any company, member or non-member, to use the Camera Link logo with any products that the company will self-certify to be compliant with the Camera Link standard. Licensed users of the Camera Link logo will not be required to credit the AIA with ownership of the registered mark.

3M™ is a trademark of the 3M Company.

Channel Link™ is a trademark of National Semiconductor.

Flatlink™ is a trademark of Texas Instruments.

Panel Link™ is a trademark of Silicon Image.

Data Port Summary

The Camera Link interface has three configurations. A single Camera Link connection is limited to 28 bits requiring some cameras to have multiple connections or channels. The naming conventions for the three configurations are:

- Base: Single Channel Link interface, single cable connector.
- Medium: Two Channel Link interface, two cable connectors.
- Full: Three Channel Link interface, two cable connectors.

A single Camera Link port is defined as having an 8-bit data word. The "Full" specification supports 8 ports labeled as A to H.

Camera Signal Summary

Video Data

Four enable signals are defined as:

- FVAL Frame Valid (FVAL) is defined HIGH for valid lines.
- LVAL Line Valid (LVAL) is defined HIGH for valid pixels.
- DVAL Data Valid (DVAL) is defined HIGH when data is valid.
- Spare A spare has been defined for future use.

All four enables must be provided by the camera on each Channel Link. All unused data bits must be tied to a known value by the camera.

Camera Controls

Four LVDS pairs are reserved for general-purpose camera control, defined as camera inputs and frame grabber outputs.

- Camera Control 1 (CC1)
- Camera Control 2 (CC2)
- Camera Control 3 (CC3)
- Camera Control 4 (CC4)

Note: the X64 Xcelera-CL LX1 by default implements the control lines as follows (using Teledyne DALSA Corporation terminology).

(CC1) EXYNC
(CC2) PRIN
(CC3) FORWARD
(CC4) HIGH

Communication

Two LVDS pairs have been allocated for asynchronous serial communication to and from the camera and frame grabber. Cameras and frame grabbers should support at least 9600 baud.

- SerTFG Differential pair with serial communications to the frame grabber.
- SerTC Differential pair with serial communications to the camera.

The serial interface protocol is one start bit, one stop bit, no parity, and no handshaking.

Camera Link Cables

For additional information on Camera Link cables and their specifications, visit the following web sites:

3M	http://www.3m.com/interconnects / *(enter Camera Link as the search keyword)*
Nortech Systems	http://www.nortechsys.com/intercon/CameraLinkMain.htm

Contact Information

Sales Information

Visit our web site: www.teledynedalsa.com/mv

Email: mailto:info@teledynedalsa.com

Canada Sales

Teledyne DALSA — Montreal office
7075 Place Robert-Joncas, Suite #142
St. Laurent, Quebec, Canada
H4M 2Z2

Tel: (514) 333-1301
Fax: (514) 333-1388

USA Sales

Teledyne DALSA — Billerica office
700 Technology Park Drive
Billerica, Ma.
01821

Tel: (978) 670-2000
Fax: (978) 670-2010

Asia Sales

Teledyne DALSA Asia Pacific
Ikebukuro East 13F
3-4-3 Higashi Ikebukuro,
Toshima-ku, Tokyo
Japan

Tel: +81 3 5960 6353
Fax: +81 3 5960 6354

European Sales

Teledyne DALSA Europe
Breslauer Str. 34
D-82194 Gröbenzell (Munich)
Germany

Tel: +49 - 8142 – 46770
Fax: +49 - 8142 – 467746

Technical Support

Any support question or request can be submitted via our web site:

Technical support form via our web page: Support requests for imaging product installations, Support requests for imaging applications	http://www.teledynedalsa.com/mv/support
Camera support information	
Product literature and driver updates	

Glossary of Terms

Bandwidth
Describes the measure of data transfer capacity. PCI devices must share the maximum PCI bus bandwidth when transferring data to and from system memory or other devices.

CAM
Sapera camera file that uses the file extension CCA by default. Files using the CCA extension, also called CAM files (CAMERA files), contain all parameters which describe the camera video signal characteristics and operation modes (that is, what the camera outputs).

Channel
Camera data path that includes all parts of a video line.

CMI
Client **M**odification **I**nstruction. A client requested engineering change applied to a Teledyne DALSA board product to support either a non-standard function or custom camera.

Contiguous memory
A block of physical memory, occupying consecutive addresses.

CRC
Proprietary Sapera raw image data file format that supports any Sapera buffer type and utilizes an informative file header. Refer to the *Sapera Basic Modules Reference Manual* "Buffer File Formats" section.

Firmware
Software such as a board driver that is stored in nonvolatile memory mounted on that board.

Frame buffer
An area of memory used to hold a frame of image data. A frame buffer may exist on the acquisition hardware or be allocated by the acquisition hardware device driver in host system memory.

Grab
Acquiring an image frame by means of a frame grabber.

Host
Refers to the computer system that supports the installed frame grabber.

Host buffer
Refers to a frame buffer allocated in the physical memory of the host computer system.

LSB
Least Significant Bit in a binary data word.

MSB
Most Significant Bit in a binary data word.

PCI Express Gen2
The PCI Express expansion bus system (PCIe) is used in consumer, server, and industrial applications, both as a motherboard-level interconnect (to link motherboard-mounted peripherals) and for computer add-in boards. Gen2 (generation 2) defines a PCIe system with double the data transfer capacity.

Pixel
Picture Element. The number of pixels describes the number of digital samples taken of the analog video signal. The number of pixels per video line by the number of active video lines describes the acquisition image resolution. The binary size of each pixel (that is, 8-bits, 15-bits, 24-bits) defines the number of gray levels or colors possible for each pixel.

RAW
A Sapera data file format where there is no header information and that supports any Sapera buffer type. Refer to the *Sapera Basic Modules Reference Manual* "Buffer File Formats" section.

Scatter Gather
Host system memory allocated for frame buffers that is virtually contiguous but physically scattered throughout all available memory.

Tap
Data path from a camera that includes a part of or whole video line. When a camera tap outputs a partial video line, the multiple camera tap data must be constructed by combining the data in the correct order.

VIC
Sapera camera parameter definition file that uses the file extension CVI by default. Files using the CVI extension, also know as VIC files, contain all operating parameters related to the frame grabber board (that is, what the frame grabber can actually do with camera controls or incoming video).

Index